# Phase Noise and Frequency Stability of the Red-Pitaya Internal PLL

A. C. Cárdenas Olaya[▽], C. E. Calosso[▽], J.-M. Friedt[∃], S. Micalizio[▽], and E. Rubiola[∃▽], *Member, IEEE*

***Abstract*—In Field Programmable Gate Array platforms, the main clock is generally a low-cost quartz oscillator whose stability is of the order of $10^{-9}$ to $10^{-10}$ in the short term and $10^{-7}$ to $10^{-8}$ in the medium term, with uncertainty of tens of ppm. Better stability is achieved by feeding an external reference into the internal PLL. We report the noise characterization of the internal PLL of Red-Pitaya platform, an open-source embedded system architected around the Zynq 7010 System on Chip, with Analog to Digital and Digital to Analog Converters. Our experiments show that, providing an external 10 MHz reference, the PLL exhibits a residual frequency stability of $1.2 \times 10^{-12}$ at 1 s and $1.3 \times 10^{-15}$ at 4000 s, Allan deviation in 5 Hz bandwidth. These results help to predict the PLL stability as a function of frequency and power of the external reference, and provide guidelines for the design of precision instrumentation, chiefly intended for time and frequency metrology.**

***Index Terms*—Digital Electronics, Frequency Stability, FPGA, Phase Locked Loop, Phase Noise.**

## I. Introduction

EMBEDDED platforms are nowadays available, capable of processing rapidly sampled signals in real time. Therefore, new methods for time and frequency metrology have been proposed, based on digital systems. These methods take advantage of compactness and reconfigurability, simplify the calibration procedures, and reduce unwanted environmental noise [1]–[5]. Commercial platforms proved to be valuable tools for research and new applications in time and frequency metrology [6], [7].

Red-Pitaya is a commercial embedded platform that integrates a dual-channel 14-bit 125 MS/s Analog to Digital Converter (ADC), a dual-channel 14-bit 125 MS/s Digital to Analog Convert (DAC) and a Xilinx Zynq 7010 System on Chip (SoC) in a small form factor. This SoC combines the Artix-7 Field Programmable Gate Array (FPGA) with a dual core Cortex-A9 ARM that runs Linux. The entire system, with the exception of the SoC processor, works at 125 MHz clock provided by a local quartz oscillator (CXO BFBC90 from TXC Corporation). The integration of these components makes Red-Pitaya an effective and powerful option for implementing digital instrumentation in different domains [8]–[14].

Referring the input and the system timebase to a common oscillator is generally necessary to achieve the high frequency resolution required in metrology applications [15]–[18]. In these applications, accuracy and stability of the Red-Pitaya on-board oscillator are not suitable, and an external reference must to be provided. Low-noise oscillators are available, at the preferred frequencies of 5 MHz, 10 MHz and 100 MHz. Since an external frequency synthesizer is expensive and bulky, the FPGA internal Phase Locked Loop (PLL) embedded in the SoC is an appealing solution. The advantages are evident in terms of reconfigurability, compactness and cost. However, the available documentation provides no information for low phase noise applications. Different methods for PLL noise characterization have been proposed. Kroupa studied in depth the noise introduced by the different components of an analog PLL [19]. More recent works present theoretical analysis [20], simulations [21], [22] and experimental results [23], [24] on the PLL noise, mainly at frequency offsets far from the carrier, and intended to provide guidelines for the design of digital PLLs. A further work [25] studied the ultimate limits of White Rabbit, a time distribution system, reporting the noise contribution of the PLLs involved in the generation of the internal clock synchronization signals.

This work focuses on the residual frequency stability of the PLL embedded into the Red-Pitaya SoC and presents the characterization of the phase noise as a function of the power and the frequency of the external reference. Our analysis enables to predict the noise contribution of the PLL in a wide range of operating conditions.

## II. Characterization Method

The scheme of the PLL internal to the Zynq 7010 [26] is shown in Fig. 1. The Voltage Controlled Oscillator (VCO) works between 800 MHz and 1.6 GHz and generates eight output signals each one with an independent counter (indicated in the Fig. 1 as $O$, $O'$, $O$", ...). The Phase and Frequency Detector (PFD) provides a signal proportional to the phase and frequency difference between the input ($\nu_i/D$) and the feedback signal ($\nu_{\rm vco}/M$). The VCO is then driven by the voltage generated by the PFD through the Charge Pump (CP) and the loop filter [23], [27]. Under lock condition, the output frequency is given by $\nu_o = \frac{M}{DO}\nu_i$, where the three parameters: $M$, $D$ and $O$ can be configured by the user. The minimum input frequency is fixed by the FPGA specifications and, for this SoC, is 10 MHz.

The phase noise of the PLL $\varphi(t)$ is represented in the frequency domain through its power spectral density (PSD) $S_\varphi(f)$. Alternatively, phase noise is expressed as phase-time fluctuations $\mathrm{x}(t)$, i.e. random phase fluctuations converted into time (1) and its corresponding PSD $S_{\mathrm{x}}(f)$.

$$\mathrm{x}(t) = \frac{\varphi(t)}{2\pi\nu_i} \tag{1}$$

▽ Physics Metrology Division, Istituto Nazionale di Ricerca Metrologica INRiM, Torino, Italy.

∃ FEMTO-ST Institute, ENSMM site, Dept. of Time and Frequency, and Université de Bourgogne and Franche-Comté (UBFC), and CNRS.

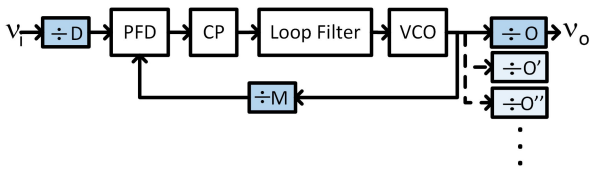



Fig. 1: PLL block diagram. Scheme of Xilinx FPGA Internal PLL.

An useful model to describe the phase noise is the polynomial law (2), which allows identifying the different noise processes through the coefficients $\mathsf{b}_j$ and $\mathsf{k}_j$. The value of $m < 0$ can be -4 or more negative for oscillators, but it is generally limited to -1 for two-port components.

$$S_\varphi(f) = \sum_{j=m}^{0} \mathsf{b}_j f^j \qquad S_\mathsf{x}(f) = \sum_{j=m}^{0} \mathsf{k}_j f^j \tag{2}$$

Here we consider two main noise sources: voltage noise $n(t)$ of the input threshold and time noise $\mathsf{x}(t)$ induced by the delay fluctuations of the logical gates along the propagation path of the PLL [28].

The PSD of $n(t)$ is represented through the polynomial law as

$$S_v(f) = \sum_{j=m}^{0} \mathrm{h}_j f^j \tag{3}$$

These voltage fluctuations generate time noise related to the input slew rate (SR), $\mathsf{x}(t) = n(t)/\mathrm{SR}$, which is expressed in phase noise by using (1). For a sinusoidal input $v_i(t) = V_i \cos(2\pi\nu_i t)$, the contribution of $n(t)$ is given by $\varphi_n(t) = \frac{n(t)}{V_i}$.

The total phase noise at the PLL input is then

$$\varphi(t) = \varphi_n(t) + \varphi_\mathsf{x}(t) = \frac{n(t)}{V_i} + 2\pi\nu_i \mathsf{x}(t) \tag{4}$$

The noise processes, $n(t)$ and $\mathsf{x}(t)$, are sampled at $2\nu_i$, in correspondence with the rising and falling zero crossings, leading to a Nyquist bandwidth of $\nu_i$. In digital electronics the analog bandwidth $B$ is higher than the maximum $\nu_i$ therefore the Nyquist theorem is not satisfied in the general case thereby occuring aliasing. As consequence, the phase white noise floor is degraded by a factor of $B/\nu_i$, while the flicker level is unaffected by the sampling process [28].

Hence, the phase noise induced by $n(t)$ and $\mathsf{x}(t)$, reported at the PLL output, the point of interest, is stated in (5) and (6) respectively, where the coefficients $\mathrm{h}_j$ and $\mathsf{k}_j$ are technical parameters of the device.

$$S_{\varphi,n}(f) = \frac{\nu_o^2}{\nu_i^2 V_i^2}\left(\frac{B\mathrm{h}_0}{\nu_i} + \sum_{j=m}^{-1} \mathrm{h}_j f^j\right) \tag{5}$$

$$S_{\varphi,\mathsf{x}}(f) = 4\pi^2\nu_o^2\left(\frac{B\mathsf{k}_0}{\nu_i} + \sum_{j=m}^{-1} \mathsf{k}_j f^j\right) \tag{6}$$

Based on this model, the PLL noise $S_\varphi = S_{\varphi,n} + S_{\varphi,\mathsf{x}}$, in particular its dependence with respect to input slew rate, is studied by changing the input carrier frequency and power.

The proposed method for extracting the PLL noise is shown in Fig. 2 and is based on the 5125A phasemeter from Symmetricom (now Microsemi). It measures the residual phase noise of the PLL by comparing directly the PLL output with the input (respectively IN and REF in Fig. 2), thus rejecting the noise of the synthesizer (Rohde & Swartz SMA-100) that is in common mode. The phasemeter accepts different frequencies by sampling the input waveforms and retrieving their phase with respect to internal numerical controlled oscillators that, in turn, are tuned to the two input frequencies respectively. Then the REF phase is scaled to the IN frequency and subtracted to the IN phase. In this manner, the residual phase noise of the PLL is directly retrieved. The noise of the common mode signal has a negligible effect to the measure since its phase noise is lower than the PLL noise for Fourier frequencies higher than 2 Hz [29]. For lower frequencies, it is rejected thanks to the common mode rejection ratio of the phasemeter ($>10^4$).

Although Red-Pitaya does not feature a dedicated connector for an external clock, the printed circuit board is predisposed for accepting it. Thus, hardware modifications were performed for providing the external reference (PLL input) through one of the extension connectors.

It is expected that the intrinsic noise of the FPGA (input and output stages) does not limit the PLL output stability. However, the phase noise of the FPGA has been evaluated and measured by bypassing the PLL.

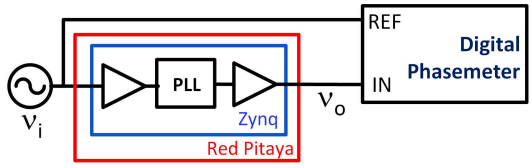



Fig. 2: Test bench for measuring the residual phase noise of the PLL. The phasemeter (Symmetricom 5125A) accepts different frequencies and rejects the noise of the synthesizer that drives the PLL.

## III. Results

The objective is to characterize the PLL noise, in particular its residual frequency stability when it generates the timebase of the digital system (FPGA, ADCs and DACs) from a high-performance external reference. For this reason, the PLL output is fixed to 125 MHz that is the system clock of Red-Pitaya. The PLL is configured for having the highest possible frequency at the input of the PFD ($D = 1$) and the VCO is set for delivering a frequency close to 1 GHz for almost all the measurements. The different PLL configurations used for the experiments are reported in Table I. Except when otherwise specified, the input power is set at 10 dBm ($V_i$ = 1 V).

The results of the phase noise characterization reported here, are focused on the flicker region, since the performance at

TABLE I: PLL configuration for obtaining 125 MHz as output frequency ($\nu_o$) from different input frequency values ($\nu_i$).

| $\nu_i$ [MHz] | $M$ | $O$ |
|---|---|---|
| 10 | 50 | 4 |
| 20 | 50 | 8 |
| 40 | 25 | 8 |
| 80 | 11 | 7 |
| 100 | 10 | 8 |
| 125 | 8 | 8 |
| 160 | 7 | 9 |

frequency offsets close to the carrier is of particular interest for time and frequency applications.

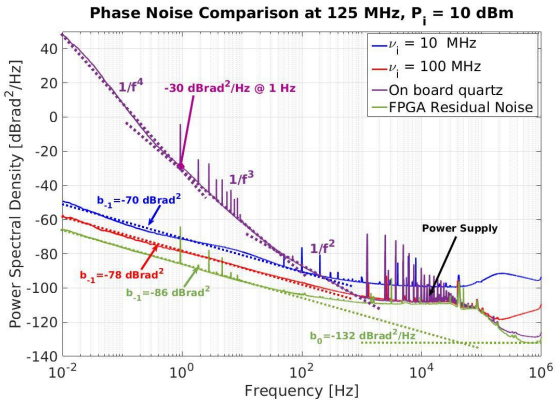
In the first experiment, we quantify the improvement that can be achieved by using an external reference. Fig. 3 compares the phase PSD (a) and the Allan deviation (b) of the on-board crystal oscillator (violet) with the residual phase noise of the PLL driven by 10 MHz (blue) and 100 MHz (red) and with the residual noise of the FPGA (green).

The phase noise at 1 Hz improves with respect to the on-board oscillator from −30 to −70 , −78 and −86 dBrad$^2$/Hz for the 10 MHz and 100 MHz PLL inputs, and the FPGA (no PLL) respectively. Similarly, the Allan deviation improved by 2-3 orders of magnitude at 1 s and by 7-8 orders of magnitude at 4000 s. This means, in case the PLL is locked to 10 MHz (the most diffused and, at the same time, the worst case) a residual frequency stability of $1.2 \times 10^{-12}$ and $1.3 \times 10^{-15}$ at 1 s and 4000 s respectively. The frequency error of Red-Pitaya oscillator is reduced by ten orders of magnitude, from 50 ppm to few parts in $10^{-15}$.

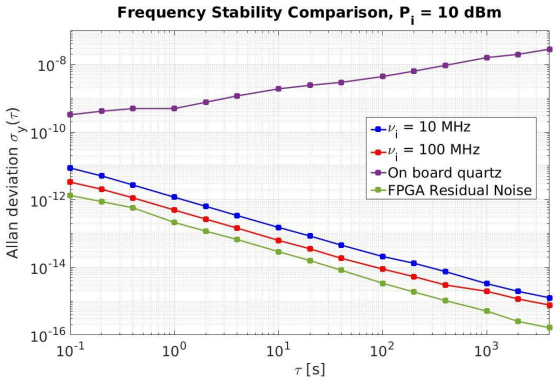
In the two experiments reported below, the input slew rate is changed by acting on the input power and on the carrier frequency independently.

First, it is assessed the performance of the PLL with respect to the input power $P_i$. It is done by increasing $P_i$ in factors of two, for two input frequencies: 10 MHz and 100 MHz. At $\nu_i$ = 10 MHz (Fig. 4a), the flicker phase noise of the PLL scales inversely with the input power ($\sim 1/V_i^2$) and this indicates that the additive noise of the input stage dominates. By using (5) we infer that $\sqrt{\mathsf{h}_{-1}}$ = 25 µV. By contrast, for $\nu_i$ = 100 MHz (Fig. 4b) the noise is independent of the input power because of a significantly higher slew rate. It suggests that at higher frequencies the noise is dominated by the time fluctuations of the PLL delay and therefore from (6) we can estimate the flicker component of $\mathsf{x}(t)$ that is $\sqrt{\mathsf{k}_{-1}} = 160$ fs.

Finally, the input carrier frequency $\nu_i$ is changed in powers of two at a fixed input power ($V_i$ = 1 V). The PSD of the PLL output phase noise is reported in Fig. 5c. At low $\nu_i$, the noise improves by increasing the input frequency, according to (5), since the noise is dominated by the additive noise of the PLL input stage. Then, an asymptotic value is reached when the noise is dominated by the time noise according to (6). The cross-over frequency, $\nu_c = \frac{1}{2\pi V_i}\frac{\sqrt{\mathsf{h}_{-1}}}{\sqrt{\mathsf{k}_{-1}}}$, is 25 MHz for $V_i$ = 1 V that corresponds to a slew rate of 156 V/µs. Fig. 5a depicts the behavior of the parameter $\mathsf{b}_{-1}$ with respect to the input frequency. Such a parameter describes the flicker phase noise of the PLL induced by voltage noise and time noise. The canonical form of $\mathsf{b}_{-1}$ [28] is observed when the noise




(a) Phase noise spectrum.




(b) Residual frequency stability. Measurement bandwidth ($f_H$) set at 5 Hz.

Fig. 3: Noise comparison between the Red-Pitaya on board quartz (violet) and the PLL driven by 10 MHz (blue) and 100 MHz (red). The residual noise of the FPGA (green) is negligible and does not affect the measure of the PLL.

is reported at the PLL input (Fig. 5b).

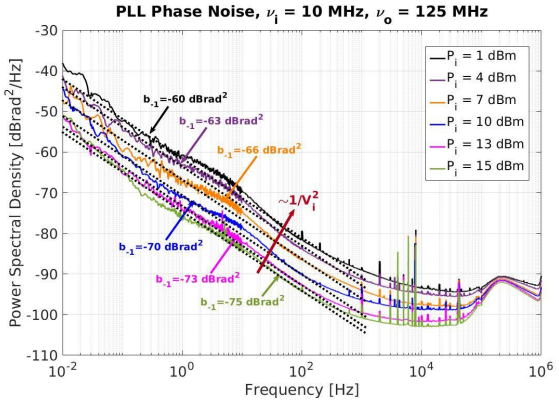
Table II reports the parameters, $\sqrt{\mathsf{h}_{-1}}$ and $\sqrt{\mathsf{k}_{-1}}$, obtained from the phase noise spectra by using the noise model stated in (5) and in (6). With this information the phase noise effects of the PLL under different operating conditions can be predicted.

TABLE II: PLL noise parameters.

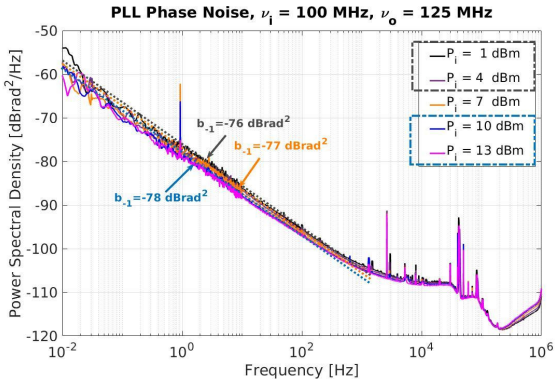
| **Parameter** | **Square Root Value PLL Zynq 7010** |
|---|---|
| $\mathsf{h}_{-1} = \frac{\nu_i^2 V_i^2}{\nu_o^2}\mathsf{b}_{-1}$, $\nu_i < \nu_c$ [a] | $\sqrt{\mathsf{h}_{-1}} = 25$ µV |
| $\mathsf{k}_{-1} = \frac{1}{4\pi^2\nu_o^2}\mathsf{b}_{-1}$, $\nu_i > \nu_c$ | $\sqrt{\mathsf{k}_{-1}} = 160$ fs |

[a] $\nu_c = \frac{1}{2\pi V_i}\frac{\sqrt{\mathsf{h}_{-1}}}{\sqrt{\mathsf{k}_{-1}}}$

For instance, if the PLL is used to generate 250 MHz from a 10 MHz reference with $V_i$ = 1 V, the flicker phase noise will be $\mathsf{b}_{-1} = -64$ dBrad$^2$. If, instead of the 10 MHz, a reference of 100 MHz is used, the flicker will be $\mathsf{b}_{-1} = -72$ dBrad$^2$. Then, the proper reference may be selected according to the application requirements. Although this noise cannot be considered the state of the art for what concerns frequency synthesis, it is adequate for many applications that, in turn,

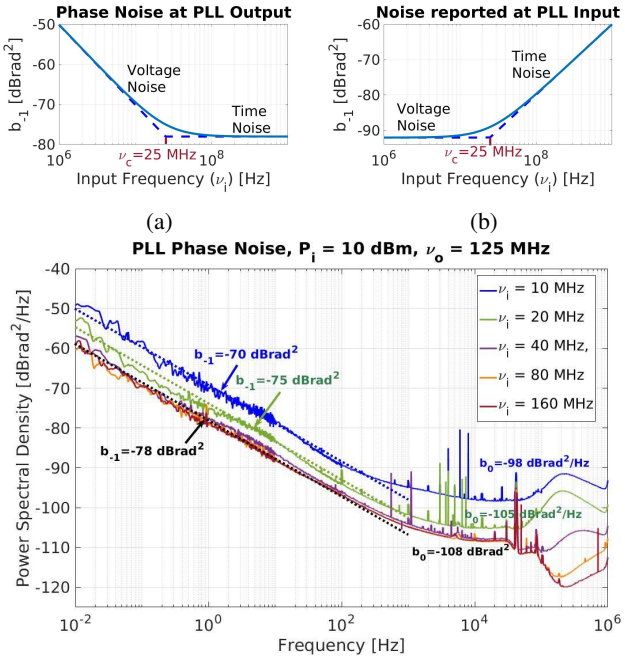



(a) $\nu_i$ = 10 MHz.




(b) $\nu_i$ = 100 MHz.

Fig. 4: PLL phase noise. The input slew rate is swept by increasing $P_i$ in factors of two for two input carrier frequencies: 10 MHz and 100 MHz.




(a) (b)

(c)

Fig. 5: PLL phase noise. The input slew rate is swept by changing $\nu_i$ in powers of two at a fixed amplitude. a) Behavior of the parameter $\mathsf{b}_{-1}$ with respect to the input frequency and reported at the PLL output. b) Canonical form of $\mathsf{b}_{-1}$. Phase noise reported at PLL input. c) Phase noise PSD of PLL output.

can take advantages of having a synthesizer embedded directly in the digital system.

## IV. Conclusion

We have characterized the internal PLL of Red-Pitaya platform for what concerns the aspects of interest for time and frequency metrology. The two noise contributions, $n(t)$ and $\mathsf{x}(t)$, were discriminated by independently sweeping the input power and carrier frequency and were quantified in $\sqrt{\mathsf{h}_{-1}} = 25\,\mu\text{V}$ and $\sqrt{\mathsf{k}_{-1}} = 160\,\text{fs}$ respectively. Best performance, in terms of phase noise, can be achieved when the slew rate of the PLL reference is higher than 156 V/µs, because the contribution of the input-stage threshold becomes negligible with respect to the time fluctuations of the PLL path.

The method presented here is general and can be applied to other PLLs, like the one embedded into the Cyclone III and whose noise was measured in [28]. In that case, this method returns $\sqrt{\mathsf{h}_{-1}} = 13\,\mu\text{V}$ and $\sqrt{\mathsf{k}_{-1}} = 140\,\text{fs}$. By considering these parameters, we observe that the time noise is very similar in the two PLLs, while the voltage noise is lower by a factor two in the Cyclone III.

To conclude, the internal PLL is a flexible solution whose frequency stability, $1.2 \times 10^{-12}$ at 1 s for a 10 MHz reference ($f_H = 5\,\text{Hz}$), is suitable for most time and frequency applications. One remarkable example is represented by frequency dissemination over fiber links. Optical fiber links have been demonstrated to reach frequency stability levels lower than $10^{-17}$ at 1 s [30]. Due to the leaverage between RF and optical frequencies, the limitation set by the PLL is expected to be at a level below $10^{-18}$ at 1 s.

## Acknowledgment

This work has been funded by the EMRP program (IND55 Mclocks). The EMRP is jointly funded by the EMRP participating countries within EURAMET and the European Union. This work has been partly supported by the ANR Programme d'Investissement dAvenir (Equipex Oscillator IMP, and Labex First-TF), and by the Region Bourgogne Franche-Comté.

## References

[1] J. Mitola III, *Software Radio Architecture: Object-Oriented Approaches to Wireless Systems Engineering*, New York, NY, USA: John Wiley & Sons, Inc., 2000.

[2] C.E. Calosso, *Tracking DDS in Time and Frequency Metrology*, Prague, Czech Republic: In Proc. of Joint European Frequency and Time Forum and International Frequency Control Symposium, 21-25 July, 2013.

[3] K. Mochizuki, M. Uchino and T. Morikawa, *Frequency-Stability Measurement System Using High-Speed ADCs and Digital Signal Processing*, IEEE Trans. Instrumentation and Measurement, Oct. 2007, **56(5)**.

[4] M. Kazda, V. Gerginov, N. Huntemann, B. Lipphardt and S. Weyers, *Phase Analysis for Frequency Standards in the Microwave and Optical Domains*, IEEE Transactions on Ultrasonics, Ferroelectrics, and Frequency Control, July 2016, **63(7)**.

[5] C.E. Calosso, E.K. Bertacco, D. Calonico, F. Levi, S. Micalizio, A. Mura, C. Clivati and G.A. Costanzo, *Tracking DDS for Coherent Optical Links*, Prague, Czech Republic: In Proc. of Joint European Frequency and Time Forum and International Frequency Control Symposium, 21-25 July, 2013.

[6] J.A. Sherman and R. Jördens, *Oscillator metrology with software defined radio*, Review of Scientific Instruments, 2016, **87**.

[7] R.A.R. Picone, S. Davis, C. Devine, J.L. Garbini and J.A. Sidles, *Instrumentation and control of harmonic oscillators via a single-board microprocessor-FPGA device*, Review of Scientific Instruments, 2017, **88(4)**.

[8] A. Tourigny-Plante, V. Michaud-Belleau, N. Bourbeau-Hébert, H. Bergeron, J. Genest and J.-D. Deschênes, *An open and flexible digital phase-locked loop for optical metrology*, Review of Scientific Instruments, 2018, **89(9)**.

[9] C. Liu, B. Tuzson, P. Scheidegger, H. Looser, B. Bereiter, M. Graf, M. Hundt, O. Aseev, D. Maas and L. Emmenegger, *Laser driving and data processing concept for mobile trace gas sensing: Design and implementation*, Review of Scientific Instruments, 2018, **89(6)**.

[10] A. Bourjilat, D. Kourtiche, F. Sarry and M. Nadi, *Interdigitated Electrode Biosensor for DNA Sequences Detection*, Casablanca, Morocco: In Proc. of 2015 27th International Conference on Microelectronics (ICM), 20-23 December, 2015.

[11] Z. Xu, J. Yao, Z. Wang, Y. Liu, H. Wang, B. Chen and H. Wu, *Development of a Portable Electrical Impedance Tomography System for Biomedical Applications*, IEEE Sensors Journal, 2018, Early Access Articles.

[12] A. Hommes, A. Shoykhetbrod, T. Geibig and P. Knott, *RAWIS support RADAR*, Prague, Czech Republic: In Proc. of 2017 18th International Radar Symposium (IRS), 28-30 June, 2017.

[13] B. Talavera and D. Cazar, *Development of a testing environment for particle detectors used by the LAGO Project*, Salinas, Ecuador: In Proc. of 2017 IEEE Second Ecuador Technical Chapters Meeting (ETCM), 16-20 October, 2017.

[14] C.J. García-Orellana, M. Macías-Macías, H. González-Velasco, A. García-Manso and R. Gallardo-Caballero, *Remote laboratory experiments of Analog Electronics based on 'RedPitaya'*, Seville, Spain: In Proc. of 2016 Technologies Applied to Electronics Teaching (TAEE), 22-24 June, 2016.

[15] S.M. Foreman, K.W. Holman, D.D. Hudson, D.J. Jones and J. Ye, *Remote transfer of ultrastable frequency references via fiber networks*, Review of Scientific Instruments, February 2007, **78**.

[16] J. Grotti *et al.*, *Geodesy and metrology with a transportable optical clock*, arXiv:1705.04089v1 [physics.atom-ph], May, 2017.

[17] C. Clivati *et al.*, *A VLBI experiment using a remote atomic clock via a coherent fibre link*, Scientific Reports, February 2017, **7**.

[18] C. Lisdat *et al.*, *A clock network for geodesy and fundamental science*, Nature Communications, August 2016, **7**.

[19] V.F. Kroupa, *Noise Properties of PLL Systems*, IEEE Transactions on Communications, October 1982, **30(10)**.

[20] A. Demir, *Computing Timing Jitter From Phase Noise Spectra for Oscillators and Phase-Locked Loops with White and 1/f Noise*, IEEE Transactions on Circuits and Systems-I, September 2006, **53(9)**.

[21] A. Boyer, S. Ben-Dhia, B. Li, C. Lemoine and B. Vrignon, *Prediction of Long-term Immunity of a Phase-Locked Loop*, Journal of Electronic Testing, December 2012, **28(6)**.

[22] A. Mehrotra, *Noise Analysis of Phase-Locked Loops*, San Jose, California, USA: In Proc. 2000 IEEE/ACM international conference on Computer-aided design, 5-9 November, 2000.

[23] M. Hsieh, J. Welch and G.E. Sobelman, *PLL performance comparison with application to spread spectrum clock generator design*, Analog Integrated Circuits and Signal Processing, May 2010, **63(2)**.

[24] F. Lei and M. H. White, *A Study of the Low Frequency Noise (LFN) in Reference Injected Phase Locked Loops (PLL-RI)*, Arlington, TX, USA: In Proc. 2016 IEEE Dallas Circuits and Systems Conference (DCAS), 10 October, 2016.

[25] M. Rizzi, M. Lipinski, P. Ferrari, S. Rinaldi and A. Flammini, *White Rabbit Clock Synchronization: Ultimate Limits on Close-In Phase Noise and Short-Term Stability due to FPGA Implementation*, IEEE Trans. on Ultrasonics, Ferroelectrics, and Frequency Control, Sept. 2018 **65(9)**.

[26] Xilinx Inc., *Technical Documentation, 7 Series FPGAs Clocking Resources*, 2018. https://www.xilinx.com/support/documentation/user_guides/ug472_7Series_Clocking.pdf

[27] Analog Devices Inc., *Technical Documentation, Fundamentals of Phase Locked Loops (PLLs)*, MT-086 Tutorial, 2009. http://www.analog.com/media/ru/training-seminars/tutorials/MT-086.pdf

[28] C.E. Calosso and E. Rubiola, *Phase Noise and Jitter in Digital Electronics*, arXiv:1701.00094 [physics.ins-det], 2016.

[29] Rohde & Schwarz, *Technical Documentation, R&S SMA100A Signal Generator Specifications*, 2013. https://cdn.rohde-schwarz.com/pws/dl_downloads/dl_common_library/dl_brochures_and_datasheets/pdf_1/SMA100A_dat-sw_en_5213-6412-22_v0700.pdf

[30] K. Predehl *et al.*, *A 920-kilometer Optical Fiber Link for Frequency Metrology at the 19th Decimal Place*, Science, April 2012, **336(6080)**.

**Andrea Carolina Cárdenas Olaya** Biography text here.

**Claudio Eligio Calosso** Biography text here.

**Jean Michel Friedt** Biography text here.

**Salvatore Micalizio** Biography text here.

**Enrico Rubiola** Biography text here.