Design and development of a surface-electrode ion trap for optical frequency metrology

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We report on the ongoing realization of a compact optical ^{171}Yb^{+} clock on a chip. The targeted fractional frequency stability is $10^{-14}\tau^{-1/2}$ for a total volume of less than 500 L, including vacuum cell, optics and electronics. Such a compact clock would be part of the growing European optical clocks network that already triggers new applications in a large variety of domains, ranging from relativistic geodesy to fundamental science [1, 2].

Four lasers at 370, 398, 638 and 935 nm are needed for ionization, cooling and repumping, see Fig. 1. They are frequency controlled using a single wavelength meter with an accuracy of 60 MHz and a frequency drift of 20 MHz/day [3].

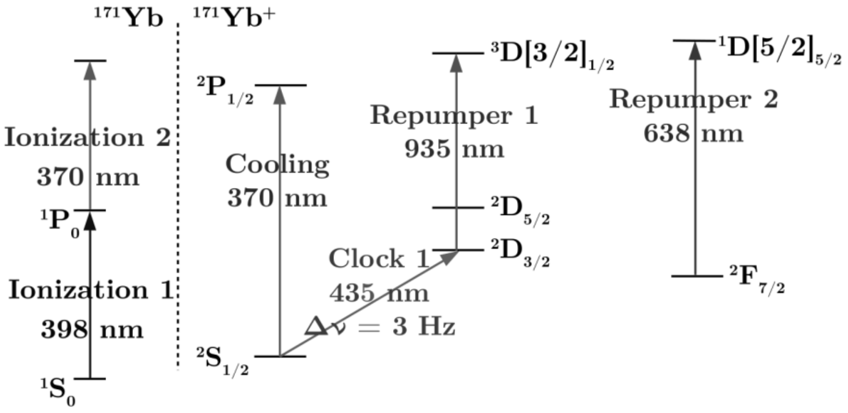

Fig. 1 Relevant atomic levels of ^{171}Yb and ^{171}Yb^{+}.

The quadrupole clock transition of ^{171}Yb^{+} at 435.5 nm will be excited using a frequency-doubled laser diode at 871 nm. We have characterized the phase noise induced by the second harmonic generation modules with a Mach-Zehnder interferometer and observed a relative phase noise as low as -40 dBrad^{2}/Hz at 1 Hz, which makes them compatible with the best up-to-date optical clocks and ultra-stable cavities [4]. The compact reference cavity at 871 nm will be based on a 2.5 cm long Fabry-Perot resonator embedded in a compact setup [5].

The experiment control essentially relies on compact home-built digital electronics.

The ion trap is based on a surface-electrode linear Paul trap. It follows the “five wires” design and microfabrication techniques that have been primarily developed and used by the quantum information community [6]. It relies on two planar RF electrodes driven at 5.8 MHz and 190 V that generate a linear Paul trap of 300 meV depth and harmonic trapping frequencies of 360 kHz radially and 100 kHz axially. The ions are trapped 500 µm from the surface.

The current chip is 30×60 mm^{2} large and has a mini-SD connector in order to allow fast plug-and-play replacements [7], see Fig. 2. This prototype trap is based on a PCB board, but the next version will take advantage of standard cleanroom microfabrication techniques.

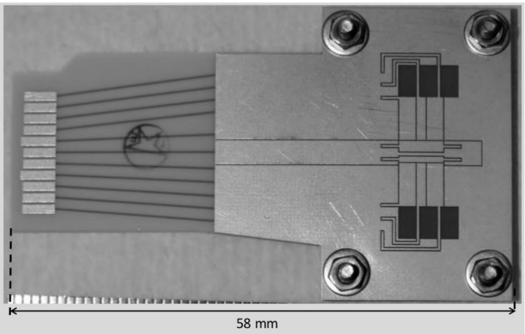

Fig. 2 Photograph of the trapping chip. It is driven at 5.8 MHz and 190 V to generate a linear Paul trap with 300 meV depth. The trapping electrodes are located on the right-hand side, while the micro-SD format on the left-hand side is used for electrical connection.

We recently demonstrated trapping of Yb^+ ions in this prototype trap (see Fig. 3), which will let us validate the proper operation of our optical setup, control electronics, and characterize our chamber base pressure. We will present the first characterization of our trap, including ion temperature, lifetime and heating rate measurements.

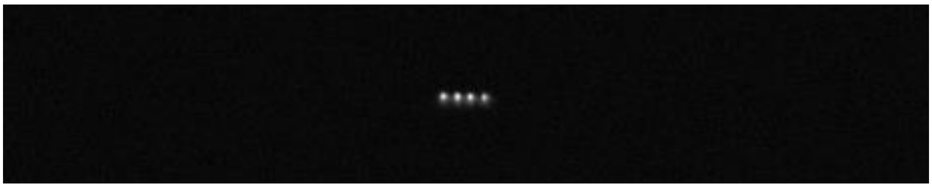

Fig. 3 Fluorescence image of a linear crystal of four $^{176}Yb^+$ ions in our prototype trap. The spacing between the ions is roughly 16 µm.

References

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