Noise Characterization of Red Pitaya Internal PLL

A. C. Cardenas-Olaya[1,2], C. E. Calosso[1], J.-M. Friedt[2], S. Micalizio[1], E. Rubiola[2]

[1]Istituto Nazionale di Ricerca Metrologica (INRiM), Physics Metrology Division, Turin, Italy
[2]Femto-ST Institute, Time and Frequency Department, Besancon, France

Email: carolina.cardenas@femto-st.fr

Increasing development on electronic technology has resulted in embedded platforms capable of performing digital processing on rapidly sampled signals allowing the use of Software Defined Radio [1] in time and frequency metrology. As consequence, new methods have been proposed based on digital systems [2], taking advantage of the reconfiguration flexibility and compactness, reducing complex calibration procedures and unwanted environmental noise. Currently, commercially available platforms provide the main components for research on this field and they have been demonstrated to be suitable tools for the implementation of time and frequency metrology [3].
In general, for time and frequency applications it is important to refer the system timebase and the Device Under Test (DUT) to a common oscillator. Most commercial platforms based on FPGA are clocked by quartz oscillators whose accuracy and frequency stability are not suitable for many of these applications being at the level of $10^{-10} - 10^{-9}$ in the short term, $10^{-8} - 10^{-7}$ in the medium term and with an uncertainty of tens of ppm. Standard low noise oscillators are available at 5 MHz, 10 MHz and 100 MHz, but generally digital systems are clocked at higher frequencies (such as 125 MHz, 250 MHz); therefore a frequency synthesizer is necessary for generating the proper system clock. Since external commercial synthesizers are expensive and bulky, in these cases it is possible to take advantage of the internal PLL provided by the FPGA to generate the internal clock from an external frequency reference. However, the PLL phase noise could degrade the oscillator stability thereby limiting the entire system performance becoming a critical component for digital instrumentation.

In this paper we report the noise characterization of the internal PLL of Red Pitaya platform, an open source embedded system architectured around a Zynq 7010 System on Chip that integrates a dual-channel 14-bit 125 MSps Analog to Digital Converter (ADC) and a dual-channel 14-bit 125MSps Digital to Analog Convert (DAC). Through experimental data we obtain that this PLL exhibits a residual frequency stability of 1.2×10^{-12} at 1 s and 1.3×10^{-15} at 4000 s for a 10 MHz carrier frequency in a 5 Hz measurement bandwidth. The results of the characterization lead to the noise limitations of the platform as a function of the reference power and frequency and this allows predicting its contribution to the performance of a specific time and frequency application in a wide range of the PLL operating conditions giving a guideline for instrumentation design techniques.

References

[1] Mitola III, J.: “Software Radio Architecture: Object-Oriented Approaches to Wireless Systems Engineering”, John Wiley & Sons, Inc., New York, NY, USA, 2000.
[2] Calosso, C. E.: “Tracking DDS in Time and Frequency Metrology”, In Proc. of Joint European Frequency and Time Forum and International Frequency Control Symposium, Prague, Czech Republic, 21-25 July, 2013.
[3] Sherman, J.A. and Jördens, R.: “Oscillator metrology with software defined radio”, Review of Scientific Instruments, 2016, 87.