Progress on a compact Yb^+ optical clock

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We report on the ongoing realization of a compact optical $^{171}Yb^+$ clock on a chip. The targeted fractional frequency stability is $10^{-14}\tau^{-1/2}$ for a total volume of less than 500 L, including vacuum cell, optics and electronics. It will be part of the growing European optical clock network, that already triggers new applications in a large variety of domains, ranging from relativistic geodesy to fundamental science [1, 2].

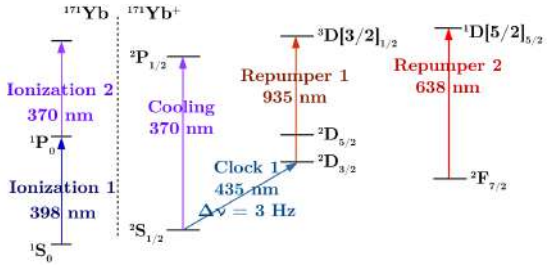

Figure 1: Relevant atomic levels of ^{171}Yb and $^{171}Yb^+$.

Four lasers at 370, 398, 638 and 935 nm are needed for ionization, cooling and repumping, see Fig. 1. They are frequency controlled using a commercial wavelength meter with an accuracy of 60 MHz and a frequency drift of 20 MHz/day [3]. The quadrupole clock transition of $^{171}Yb^+$ at 435.5 nm will be excited using a frequency-doubled laser diode at 871 nm. We have characterized the phase noise induced by the second harmonic generation modules with a Mach-Zehnder interferometer and observed a relative phase noise as low as $40\,\mathrm{dBrad^2/Hz}$ at 1 Hz, which makes them compatible with the best up-to-date optical clocks and ultra-stable cavities [4]. The compact reference cavity at 871 nm will be based on an existing design.

Experiment control is essentially made with compact home-built digital electronics.

The ion trap is based on a surface-electrode linear Paul trap. It follows the "five wires" design and microfabrication techniques that have been primarily developed and used by the quantum information community [5]. It relies on two planar RF electrodes driven at 5.8 MHz and 190 V that generate a linear Paul trap of 300 meV depth and harmonic trapping frequencies of 360 kHz radially and 100 kHz axially. The ions are trapped 500 µm from the surface. The current chip is $30 \times 60\,\mathrm{mm^2}$ large and has a mini-SD connector in order to allow fast plug-and-play replacements, see Fig. 2. It is now a PCB board,

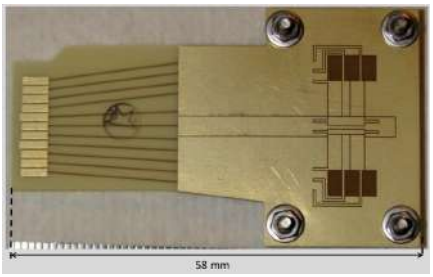

Figure 2: Photograph of the chip. It is driven at 5.8 MHz and 190 V to generate a linear Paul trap with 300 meV depth.

but the next version will take advantage of standard cleanroom microfabrication techniques.

We will present the first characterization of our trap, including including ion temperature, lifetime and heating rate measurements.

[1] C. Lisdat et al., Nat. Comm. **7**, 12443 (2016)

[2] F. Riehle, Nat. Phot. **11**, 1 (2017)

[3] K. Saleh et al., App. Opt **54**, 32 (2015)

[4] M. Delehaye et al., IEEE PTL **29**, 19 (2017)

[5] S. Seidelin et al., Phys. Rev. Lett. **96**, 25 (2006)