Robust Adaptive Control of Interleaved Boost Converter for Fuel Cell Application

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***Abstract*—In this article, a robust adaptive controller based on active disturbance rejection control algorithm is proposed for interleaved dc–dc Boost converter for fuel cell application. The unknown load power and parametric variations are regarded as part of the total disturbance, which is estimated by extended-state-observer (ESO), and then canceled in the control law. Within the proposed controller, the parameter b_0 is adapted in real-time to reduce the estimation burden of ESO. It is shown that compared with the conventional controller, the proposed controller can achieve significant improvement in terms of robustness, the strong antidisturbance performance can be maintained with the varied number of active phases. Finally, simulation and experimental results validate the effectiveness and superiority of the proposed controller.**

***Index Terms*—Antidisturbance, dc–dc power converter, fuel cell (FC) application, interleaved converter, robustness.**

I. Introduction

WITH the gradual depletion of conventional fossil energy due to the massive use and its effect on environmental change and air pollution, the new energy source, which is represented by the photovoltaic, wind turbine, and fuel cell (FC), is getting more and more research attention. Hydrogen FC is a device that converts the chemical energy stored in the hydrogen into electricity, the only byproducts are water and heat. FC has many advantages, such as high power density, silent operation, low operating temperature, and zero-emission. It has been increasingly used in portable, stationary, and transportation applications [1], [2]. However, FC is low-voltage high-current, and it features nonlinear volt-ampere characteristic, the FC voltage varies oppositely with the FC current. Therefore, it is essential to interface with a dc–dc converter to increase and regulate a stiff dc bus to satisfy the load requirement [3], [4]. The interleaved dc–dc converter is an attractive choice. With the phase interleaving operation by phase-shifting properly the switch signals, low input current ripple is allowed, being beneficial for FC long time service [5], [6]. Moreover, the FC current can be shared by the active phases of the converter, and the efficiency can be improved [7]. In addition, the interleaved converters can continue operating even after a phase goes out of service [8]. This characteristic is very important for the earlier mission-critical and safety-critical applications.

The interleaved converter for FC application suffers from parametric variations (parasitic resistance, inductance, capacitance, and number of converter active phases) and external disturbances (unknown load power, and varied FC voltage), which are the challenges for the converter controller. In [9], a double-loop proportional-integral (PI) controller consisting of the inductor current inner-loop and output voltage outer-loop is designed for the interleaved converter, to regulate the output voltage at the desired value. It is shown that the performance of PI control designed based on the nominal condition varies with the operation point. To achieve better performance with smaller steady-state error, faster dynamical response, lower overshoot, and stronger robustness, various linear and nonlinear controllers are developed. In [10] and [11], a sliding mode control is designed for the interleaved converter. To maintain the constant switching frequency and interleaving, the hysteresis of the control signal generating comparators should be adjusted dynamically, which increases the controller complexity. In [12], a passivity-based control is designed for an interleaved converter for FC application. The control law, however, requires accurate converter model information. In [13], a model predictive control is designed to deal with the uncertainties. Simulation results confirm the solid and robust performance. One limitation is that the computation burden within one switching period is a little heavy, which may be a challenge for hardware implementation.

Disturbance estimation and compensation control have been obtaining more and more research attention [14]. It shows great prospects in applications of induction motors, permanent magnet synchronous motor, air compressors, rectifiers, grid-connected inverters, etc. [15]–[20]. The principle is to estimate in real-time the uncertainties and disturbances, and then compensate them directly in the control law. One typical algorithm is the active disturbance rejection control (ADRC) [21]. It takes the single or cascade integral as the canonical form of the plant, and the

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difference between the real plant and canonical plant is treated as the total disturbance, which includes the converter uncertainties and disturbances. Then, the total disturbance is regarded as an extended state that can be estimated by extended-state-observer (ESO) in real-time based on the converter input and output variable. By compensating the estimated total disturbance to the control law, good robustness against uncertainties and disturbances can be obtained. ADRC is designed based on the canonical plant, therefore, the accurate converter model is not necessary, it only needs to obtain the system order. The original ADRC is of nonlinear form. To simplify the analysis and ease the implementation, the nonlinear gains are replaced by the linear ones to introduce the linear ADRC [22]. In [23], the ESO-based ADRC is proposed for a two-phase interleaved Boost converter for FC application. The comparison with PI control demonstrates that ADRC is more robust to the disturbances. However, be the same as that of PI control, the controller performance of ADRC would degrade when the number of converter active phases reduces to improve the light load efficiency or caused by the hard fault. It is, thus, essential to develop an improved controller with stronger robustness.

To this end, a robust adaptive controller based on the ADRC algorithm is proposed in this article for interleaved converters with unknown power load for FC application. The parametric variations (such as converter circuit parameter deviation and the reduction of the number of active phases) and unknown load power are regarded as part of the total disturbance, which could be estimated by ESO and canceled in the control law. Within the proposed controller, the system control gain b is obtained based on the input voltage, which is then used to adapt the parameter b_0 to reduce the estimation burden of ESO. Compared with the conventional ADRC, the proposed controller can achieve significant improvement with stronger robustness. The proposed method can be extended to other interleaved converters.

This article is organized as follows. The converter analysis and modeling are presented in Section II. Then, the proposed adaptive controller is elaborated in Section III. To validate the effectiveness and robustness of the proposed controller, simulation results based on MATLAB/Simulink are presented in Section IV. Furthermore, the laboratory converter prototype is built, and the proposed controllers are implemented into the dSPACE platform. Experimental results are shown in Section V. Finally, the conclusion in Section VI ends this article.

II. Converter Analysis and Modeling

A. Converter Analysis

Fig. 1 shows the topology of the N-phase interleaved Boost converter. For each phase, there is one inductor $L_k(k = 1, 2, \ldots, N)$, one switch S_k, and one diode D_k. C is the common capacitor, and r_k is the circuit lumped parasitic resistance. v_{in} is the converter input voltage, v_o is the converter output voltage, and i_o is the converter output current.

The converter input current i_{in} is given as follows:

$$i_{in} = \sum_{k=1}^{k=N} i_{Lk} \tag{1}$$

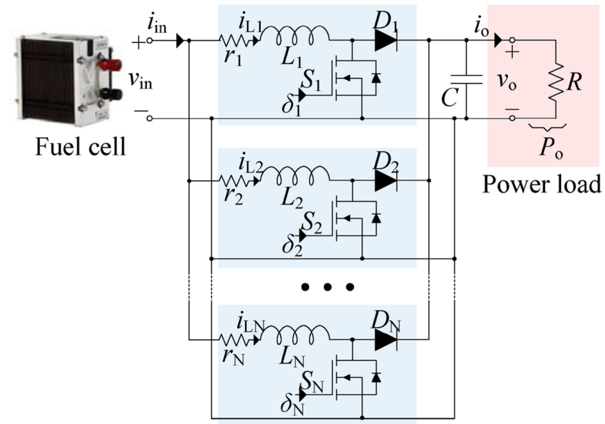


Fig. 1. N-phase interleaved Boost converter for FC application.

where $i_{Lk}(k = 1, 2, \ldots, N)$ is the current flowing through the inductor L_k. The symmetrical circuit parameters are generally considered to realize the modular design, therefore

$$L_k = L,\ r_k = r,\ \ d_k = d, k = 1, 2, \ldots, N \tag{2}$$

where d_k is the duty cycle generated by the control system for the power switch S_k.

The static voltage gain of the ideal interleaved Boost converter working in continuous conduction mode is

$$M(d) = \frac{V_o}{V_{in}} = \frac{1}{1-d} \tag{3}$$

where d is the duty cycle, and V_o and V_{in} are the dc values of the variable v_o and v_{in}, respectively.

Consider $N = 2$, according to the converter operation principle, the average model of the interleaved Boost converter is

$$\frac{d}{dt} i_{Lk} = \frac{1}{L_k} \left(v_{in} - r_k i_{Lk} - (1-d_k) v_o\right), k = 1, 2 \tag{4.a}$$

$$\frac{d}{dt} v_o = \frac{1}{C} \left(\sum_{k=1}^{k=2} (1-d_k) i_{Lk} - i_o\right) \tag{4.b}$$

where d_k $(k = 1, 2)$ is the duty cycle of the switch S_k.

B. Control Scheme

The converter for FC application suffers from load disturbance and input voltage variation. Therefore, to achieve the desired output voltage, the double-loop control structure containing the inductor current inner-loops and the output voltage outer-loop is used, as shown in Fig. 2. The outer-loop generates the current reference I_{Lref} for the inner-loops, by dealing with the voltage reference V_{ref} and output voltage v_o. Then, the inner-loops produce the duty cycles $d_k(k = 1, 2)$ to modulate the ON–OFF signal δ_k for switch S_k via pulsewidth modulation. When $\delta_k = 0$, switch S_k turns OFF, and $\delta_k = 1$, switch S_k turns ON. Notably, the switch ON–OFF signals are generally phase-shifted successively by $360°/N$ to realize the interleaved operation to reduce the input current ripple.

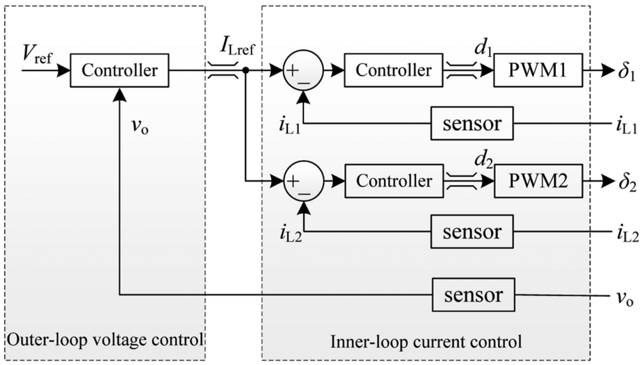


Fig. 2. Double-loop control structure.

C. Converter Modeling

The target of the inner-loop is to regulate the inductor currents to the reference value, which is produced by the outer-loop. The following super-twisting sliding mode control law [24], which is also considered as a kind of nonlinear PI control, features good robustness and tracking ability. Thus, it is adopted as the inner-loop control.

$$\begin{cases} d_k = \lambda |s_k|^{\frac{1}{2}} sign\,(s_k) + \alpha \int \mathrm{sign}\,(s_k)\, dt \\ s_k = I_{Lref} - i_{Lk}, k = 1, 2 \end{cases} \tag{5}$$

where s_k is the sliding surface, I_{Lref} is the current reference generated by the outer-loop, the sign is a standard *sign* function, and λ and α are controller parameters to be tuned.

By applying the invariance condition ($s_k = \dot{s}_k = 0$), the equivalent duty cycle can be obtained based on (4.a).

$$d_{\mathrm{eq}} = 1 - \frac{(v_{in} - r_k I_{Lref})}{v_o}. \tag{6}$$

1) Converter With Two Active Phases: Substitute $s_k = 0$ and (6) into (4.b), there is

$$\frac{dv_o}{dt} = \frac{1}{C}\left(\sum_{k=1}^{k=2} \frac{v_{in} - r_k I_{Lref}}{v_o} I_{Lref} - i_o\right). \tag{7}$$

The above-mentioned equation can be rewritten as follows, by multiplying the output voltage $v_o(v_o \geq v_{in} > 0)$ on both sides:

$$\frac{d}{dt}\left(\frac{1}{2}Cv_o^2\right) = \sum_{k=1}^{k=2} (v_{in} - r_k I_{Lref})\, I_{Lref} - i_o v_o. \tag{8}$$

Namely,

$$\underbrace{\frac{d}{dt}\left(\frac{1}{2}Cv_o^2\right)}_{E_C} = \underbrace{2v_{in}I_{Lref}}_{P_{in}} - \underbrace{(r_1 + r_2)\, I_{Lref}^2}_{P_{loss}} - \underbrace{v_o i_o}_{P_o} \tag{9}$$

where E_C is the energy stored in the capacitor, P_{in} is the converter input power from FC stack, P_{loss} is the converter power losses, and P_o is the unknown load power.

2) Converter With One Active Phase: Following the same procedure as earlier, the converter model in the case of one active phase can be derived as follows:

$$\underbrace{\frac{d}{dt}\left(\frac{1}{2}Cv_o^2\right)}_{E_C} = \underbrace{v_{in}I_{Lref}}_{P_{in}} - \underbrace{r_1 I_{Lref}^2}_{P_{loss}} - \underbrace{v_o i_o}_{P_o}. \tag{10}$$

In what follows, the outer-loop controller is designed based on the equivalent converter model (9) and (10).

III. Proposed Control Strategy

A. Voltage Controller Design

Denote $y = \frac{1}{2}Cv_o^2, u = I_{Lref}$, then the converter model (9) and (10) can be rewritten as follows:

$$\dot{y} = bu - P_{loss} - P_o = b_0\, u + f \tag{11}$$

where b is the system control gain, $f = (b - b_0)\, u - P_{loss} - P_o$ is the total disturbance to be estimated, and b_0 is the controller parameter to be tuned. The (11) can be rewritten as follows:

$$\begin{cases} \dot{x} = \underbrace{\begin{bmatrix} 0 & 1 \\ 0 & 0 \end{bmatrix}}_{A} x + \underbrace{\begin{bmatrix} b_0 \\ 0 \end{bmatrix}}_{B} u + \underbrace{\begin{bmatrix} 0 \\ 1 \end{bmatrix}}_{E} \dot{f} \\ y = \underbrace{\begin{bmatrix} 1 & 0 \end{bmatrix}}_{C}\ x \end{cases} \tag{12}$$

where the state variable $\boldsymbol{x} = [x_1\ x_2]^T = [y\ f]^T$.

To online estimate the total disturbance in real-time, the following ESO for system (12) can be designed as follows:

$$\dot{\boldsymbol{z}} = \boldsymbol{A}\boldsymbol{z} + \boldsymbol{B}u + \boldsymbol{G}e_1 \tag{13}$$

where $\boldsymbol{z} = [z_1\ z_2\ ]^T$, $\boldsymbol{G} = [g_1\ g_2]^T$, $e_1 = x_1 - z_1$ is the observer error. The tracking form is $z_1 \to x_1$, and $z_2 \to x_2$, and g_1 and g_2 are observer gains to be tuned. Generally, the bandwidth method is used to tune the observer gains, that is, $g_1 = 2\omega_o$, and $g_2 = \omega_o^2$, ω_o is the observer bandwidth [22].

Finally, the control law can be designed as follows:

$$u = \frac{u_0 - z_2}{b_0} \tag{14}$$

such that the system (11) can be simplified as an integral unit

$$\dot{y} = u_0 \tag{15}$$

supposing that the total disturbance is well-estimated by ESO. Therefore, one can use the proportional control law to regulate the output voltage.

$$u_0 = k_p\ (E_{ref} - z_1) \tag{16}$$

where $E_{ref} = \frac{1}{2}CV_{ref}^2$, V_{ref} is the voltage reference, and k_p is the controller parameter to be designed.

B. Stability Analysis

Define $\boldsymbol{e} = [e_1\ e_2\ e_3]^T$, $e_1 = x_1 - z_1$, $e_2 = x_2 - z_2$, and $e_3 = E_{ref} - x_1$, it follows from (12) and (13) that the error

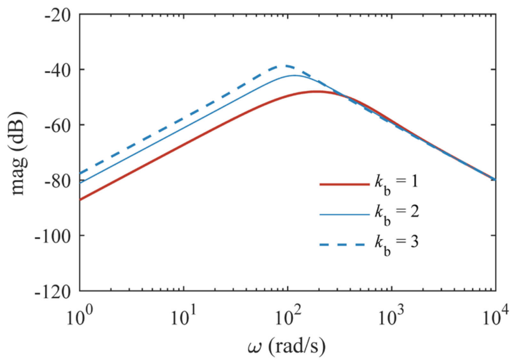


Fig. 3. Bode plot of transfer function $\phi_d(s)$, ω_o= 400, and k_p = 400/3.

dynamics are

$$\dot{\boldsymbol{e}} = \underbrace{\begin{bmatrix} -g_1 & 1 & 0 \\ -g_2 & 0 & 0 \\ -k_p & -1 & -k_p \end{bmatrix}}_{H} \boldsymbol{e} + \begin{bmatrix} 0 \\ \dot{f} \\ 0 \end{bmatrix}. \tag{17}$$

The eigenvalues of the matrix $\boldsymbol{H}$ in (17) are

$$\lambda_1 = \lambda_2 = -\omega_o, \quad \lambda_3 = -k_p \tag{18}$$

which all located in the left-half plane if ω_o and k_p are the positive number. The controller is globally asymptotically stable, and the error dynamics can converge to the equilibrium point, $\lim\limits_{t\to\infty} e_1 = 0$, $\lim\limits_{t\to\infty} e_2 = 0$, and $\lim\limits_{t\to\infty} e_3 = 0$. In steady-state, the output voltage can achieve $v_o = V_{ref}$.

C. Discussion About the Controller Parameters

As shown in (18), to ensure the controller stability, the control parameters ω_o and k_p should satisfy $\omega_o > 0$ and $k_p > 0$. The ω_o mainly influences the disturbance estimation performance of ESO. The larger ω_o leads to a faster convergence speed of the estimation, and vice versa. It needs to note that in real applications, due to the limited sampling rate of converter voltage, a too large ω_o may introduce intolerable noise to the system. Moreover, the k_p mainly influences the control speed, and generally, there is $k_p < \omega_o$.

The control parameter b_0 is very key. For the conventional controller, the b_0 is set as the nominal value of the system control gain b. However, the control gain b varies with input voltage and the number of the active phase, introducing an extra estimation burden for ESO, see (9)–(11). This phenomenon would deteriorate the controller performance in terms of disturbance rejection, as analyzed theoretically in the following.

Define $k_b = b_0/b$, then the transfer function from the disturbance to output voltage can be derived as (19), according to (11)–(16).

$$\begin{aligned} \phi_d\ (s) &= \frac{V_o\,(s)}{f\,(s)} \\ &= \frac{k_b s\,(s + g_1 + k_p)}{k_b s^2\,(s + g_1 + k_p) + (k_p g_1 + g_2)\,s + k_p g_2}. \end{aligned} \tag{19}$$

TABLE I
CONVERTER PARAMETERS

Description	Symbol	Value
Input voltage	v_{in}	16 V
Output voltage	V_{ref}	48 V
Switching frequency	f_s	25 kHz
Inductance	L	400 µH
Inductor resistance	r_L	0.40 Ω
Capacitance	C	1000 µF
Capacitor resistance	r_C	0.04 Ω

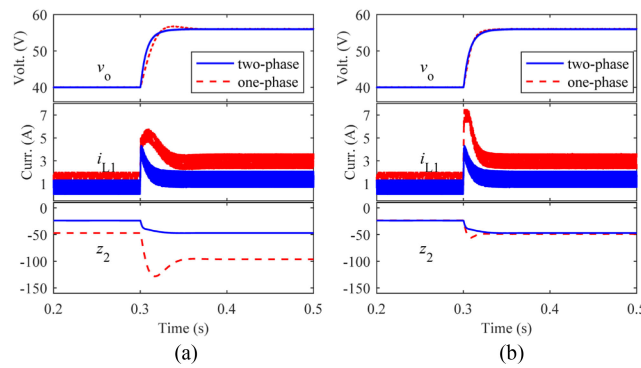


Fig. 4. Simulation results of the converter with different controllers, voltage reference V_{ref} steps from 40 to 56 V at t = 0.3 s. (a) Conventional controller. (b) Proposed controller.

Fig. 3 shows the Bode plot of (19) with k_b variation. It is seen that larger k_b would result in weaker disturbance rejection ability, as the disturbance is generally of low frequency.

In this article, we propose to adapt the parameter b_0 as $b_0 = nv_{in}$, n is the number of active phases, to track the control gain b such that $k_b \approx 1$. In this way, when the number of active phases reduces, the estimation burden of ESO would not increase, and the uncompromised disturbance rejection performance with the different number of converter active phases can be maintained.

IV. SIMULATION RESULTS

The simulation model containing a two-phase interleaved Boost converter and the controllers are established based on MATLAB/Simulink environment, the converter parameters are listed in Table I. The nonideal power switch ($r_{on} = 1$ mΩ, $V_f = 0.5$ V) and power diode ($r_{on} = 1$ mΩ, $V_f = 0.4$ V) are used. The controller parameters for inner-loop are $\lambda = 0.05$, $\alpha = 60$, and that for outer-loop are $\omega_o = 400$, $\omega_c = 60$. For the conventional controller, the parameter b_0 is set as the nominal value of system control gain, $b_0 = 32$. For the proposed controller, the parameter b_0 is adapted in real-time, as discussed in Section III.C.

A. Voltage Reference Step Response

Fig. 4 shows the simulation results when the voltage reference V_{ref} steps from 40 to 56 V. It is seen from Fig. 4(a) that for the conventional controller, there is no voltage overshoot in the case of two active phases. However, when the converter operating in one active phase, the voltage overshoot occurs. In contrast,

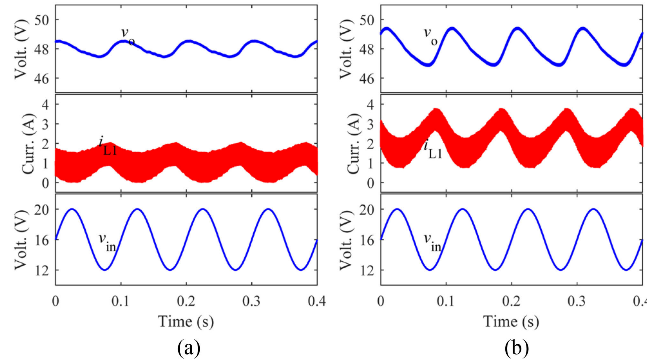


Fig. 5. Simulation results of the converter with conventional controller, input voltage $v_{in} = 16 + 4sin(20\pi t)$V. (a) Case of two active phases. (b) Case of one active phase.

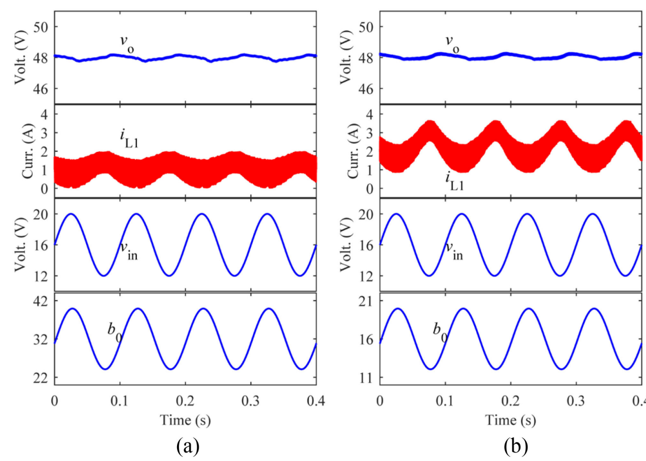


Fig. 6. Simulation results of the converter with proposed controller, input voltage $v_{in} = 16 + 4sin(20\pi t)$V. (a) Case of two active phases. (b) Case of one active phase.

for the proposed controller, the voltage response of two active phases and that of one active phase are almost consistent, there is no voltage overshoot, as can be observed in Fig. 4(b).

According to the above-mentioned analysis, both the conventional controller and proposed one can achieve good performance under two active phases. However, the proposed controller can achieve a better step response under one active phase. This is because that the proposed adaptive controller can alleviate the estimation burden (absolute value of z_2) through adapting the parameter b_0 in real-time.

B. Input Voltage Variation

Figs. 5 and 6 show, respectively, the simulation results of input voltage variation with the conventional controller and the proposed controller. The load resistance is 100 Ω and the sinusoidal input voltage of $v_{in} = 16 + 4sin(20\pi t)$V is applied to the converter. It is seen from Fig. 5(a) and (b), for the conventional controller, the output voltage fluctuation under one active phase is larger than that under two active phases, indicating that for the conventional controller, the disturbance rejection performance would deteriorate when the active phase reduces from two to one.

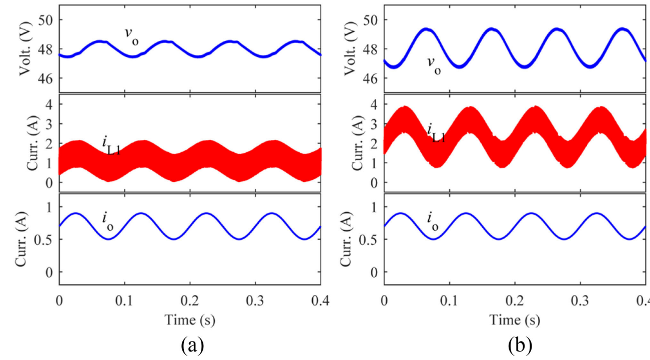


Fig. 7. Simulation results of the converter with conventional controller, load current $i_o = 0.7 + 0.2sin(20\pi t)$A. (a) Case of two active phases. (b) Case of one active phase.

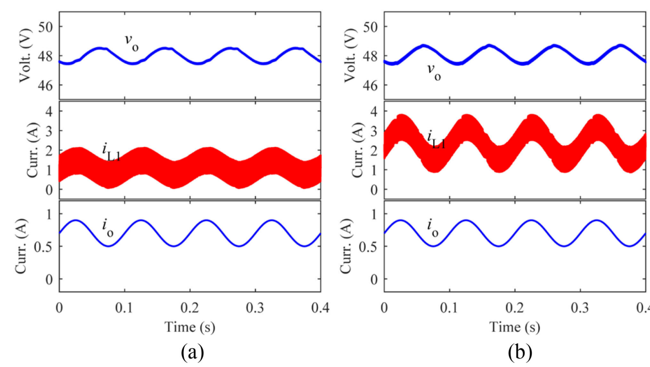


Fig. 8. Simulation results of the converter with proposed controller, load current $i_o = 0.7 + 0.2sin(20\pi t)$A. (a) Case of two active phases. (b) Case of one active phase.

In comparison, for the proposed controller with adaptive b_0, the output voltage fluctuation under one active phase is almost the same as that under two active phases, as shown in Fig. 6(a) and (b). This demonstrates that the proposed controller has better performance, the strong antidisturbance performance can be maintained under one and two active phases.

C. Load Current Disturbance

Figs. 7 and 8 present, respectively, the simulation results of load current disturbance with the conventional controller and the proposed controller. The input voltage is v_{in}= 16 V, and the sinusoidal load current disturbance of $i_o = 0.7 + 0.2sin(20\pi t)$A is applied to the converter. It is observed from Figs. 7(a) and 8(a) that when the converter operating in the mode of two active phases, the output voltage fluctuation of the conventional controller and that of the proposed controller are almost the same. However, when the converter operating in the mode of one active phase, the proposed adaptive controller can achieve better performance with smaller voltage fluctuation, see Figs. 7(b) and 8(b). The results validate that the proposed adaptive controller has stronger robustness against disturbance.

D. FC Application

To validate the feasibility of the proposed controller for FC application, a 20-cell FC stack modeled in [25] is interfaced with

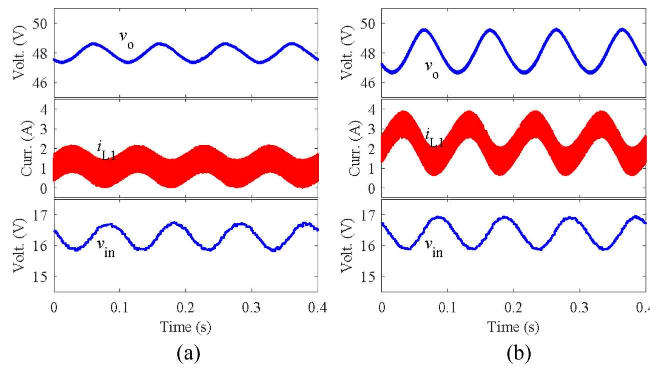


Fig. 9. Simulation results of the converter interfaced with FC stack under conventional controller, load current $i_o = 0.7 + 0.2sin(20\pi t)$A. (a) Case of two active phases. (b) Case of one active phase.

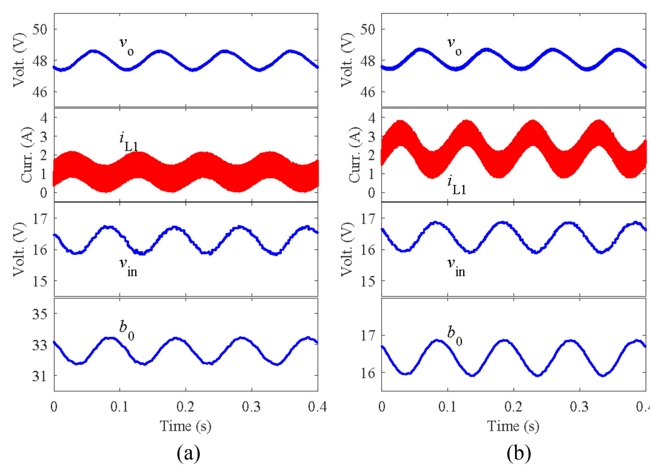


Fig. 10. Simulation results of the converter interfaced with FC stack under proposed controller, load current $i_o = 0.7 + 0.2sin(20\pi t)$A. (a) Case of two active phases. (b) Case of one active phase.

the converter. The sinusoidal load current disturbance of $i_o = 0.7 + 0.2sin(20\pi t)$A is applied, the input FC voltage varies accordingly. The results with the conventional controller and proposed one are plotted in Figs. 9 and 10, respectively. As can be seen from Figs. 9(a) and 10(a), when the converter operating in the mode of two active phases, the conventional controller and the proposed one can achieve almost consistent performance. However, when the converter operating in the mode of one active phase, the proposed controller can achieve better performance with smaller voltage fluctuation, see Figs. 9(b) and 10(b). The results validate again the stronger robustness of the proposed adaptive controller against disturbances, and the feasibility of FC application is also demonstrated.

V. Experimental Validation

To further validate the effectiveness and robustness of the proposed controller, a two-phase interleaved Boost converter prototype has been built, the converter circuit parameters are the same as in Table I. Fig. 11 shows the experimental set-up. The controllers are implemented into the dSPACE platform and the generated switch ON–OFF signals δ_1 and δ_2 are then phase-shifted by 180° via FPGA board to realize interleaved operation. The

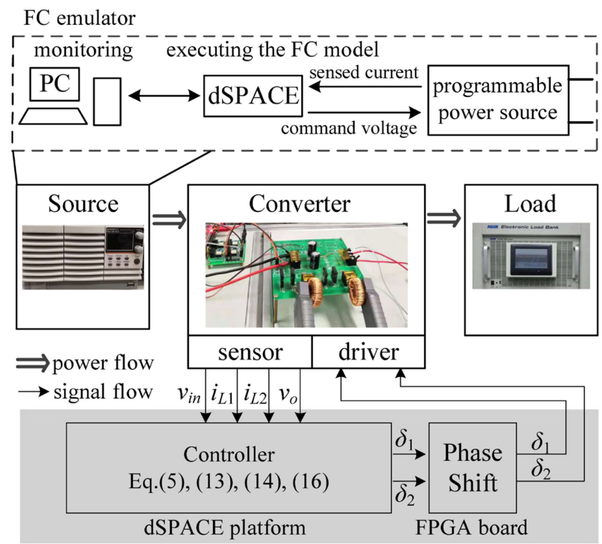


Fig. 11. Experimental set-up.

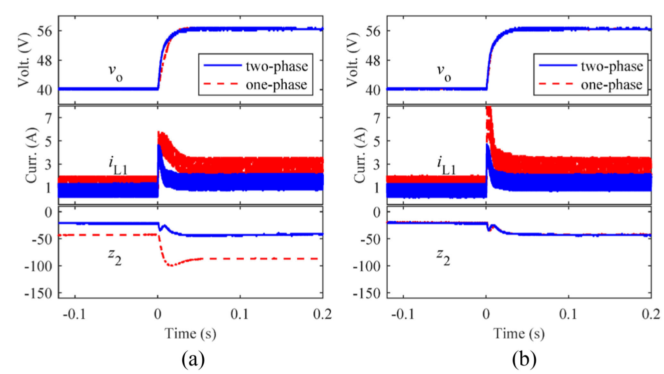


Fig. 12. Experimental results of the converter with different controllers, voltage reference V_{ref} steps from 40 to 56 V at t = 0 s. (a) Conventional controller. (b) Proposed controller.

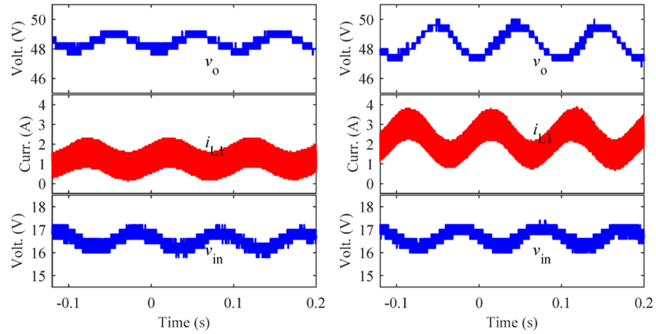
20-cell FC stack is emulated using the programmable power source. The experimental figures are plotted based on the data captured by the oscilloscope of Tektronix DPO2014B.

A. Voltage Reference Step Response

Fig. 12 presents the experimental results when the voltage reference V_{ref} steps from 40 to 56 V at t = 0 s. The load resistance is R = 100 Ω, and the input voltage is v_{in}= 16 V. It is observed that the obtained experimental results are similar to the simulation results of Fig. 4. Moreover, as shown in Fig. 12, both the conventional controller and proposed one can achieve good performance when the converter operating in the mode of two active phases. However, when converter operating in the mode of one active phase, the proposed controller can alleviate the estimation burden (absolute value of z_2) by adapting b_0, thus, a better step response can be obtained.

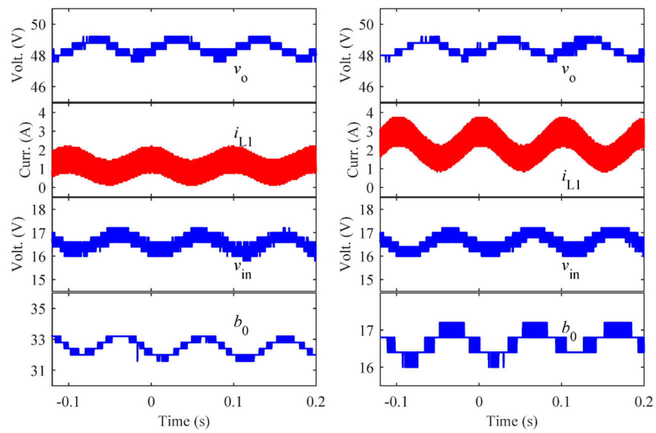
B. Load Current Sinusoidal Disturbance

Figs. 13 and 14 show, respectively, the experimental results with the conventional controller and proposed adaptive



(a) (b)

Fig. 13. Experimental results of the converter interfaced with FC stack under conventional controller, load current $i_o = 0.7 + 0.2sin(20\pi t)$A. (a) Case of two active phases. (b) Case of one active phase.



(a) (b)

Fig. 14. Experimental results of the converter interfaced with FC stack under proposed controller, load current $i_o = 0.7 + 0.2sin(20\pi t)$A. (a) Case of two active phases. (b) Case of one active phase.

controller. The converter is interfaced with a 20-cell FC stack and the load current of $i_o = 0.7 + 0.2sin(20\pi t)$A is applied to the converter. The obtained experimental results are similar to the simulation results of Figs. 9 and 10. As shown in Figs. 13(a) and 14(a), when the converter operating in the mode of two active phases, both controllers have similar performance. When the converter operating in the mode of one active phase, the proposed one can achieve better performance with smaller voltage fluctuation, see Figs. 13(b) and 14(b). It is noted that the waveform of b_0 is not as smooth as that in the simulations, this is because to export the value of b_0 to the oscilloscope, a digital-to-analog converter is used, which has limited accuracy. The experimental results validate again the stronger robustness of the proposed controller against disturbances and the feasibility of FC application.

VI. Conclusion

Due to the FC nonlinear volt-ampere characteristic, it is necessary to interface with a dc–dc converter to satisfy the load requirement. In this article, a robust adaptive controller based on the ADRC algorithm is proposed for an interleaved dc–dc Boost converter for FC application. The unknown load power and variation in the number of active phases are treated as part of the total disturbance, which is estimated by ESO and canceled in the control law. The parameter b_0 is adapted in real-time to alleviate the estimation burden of ESO. Simulation and experimental results demonstrate that in comparison with the conventional ADRC, the proposed controller can achieve stronger robustness against unknown external disturbances. Especially, the strong antidisturbance performance can be maintained with the varied number of active phases. The proposed controller can also be extended to other interleaved converters.

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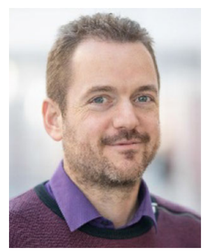

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