Lookup Table-based Electro-Thermal Real-Time Simulation of Output Series Interleaved Boost Converter for Fuel Cell Applications

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***Abstract*—Due to the high dependency between reliability of power device and its junction temperature, monitoring their thermal behavior in real time is very essential. In this paper, a lookup table-based electro-thermal real-time simulation model is developed to quickly estimate the junction temperature of the power devices. Output series interleaved boost converter with high voltage gain and low input current ripple, which is dedicated for fuel cell application, is selected as a case study. The thorough design and implementation process are presented and the developed model is simulated with a 200 nanoseconds time step on NI FlexRIO PXIe-7975R real-time platform. Moreover, the effectiveness and accuracy of the FPGA-based electro-thermal model are validated by comparison the results from PLECS software.**

Keywords—output serirs interleaved boost converter, lookup table-based electro-thermal model, real-time simulation, FPGA.

I. INTRODUCTION

As a renewable energy with zero emission, high efficiency, and high durability, fuel cell has been successfully applied to various industrial fields like transportation, aerospace and distributed generation [1] [2]. However, considering the lower output voltage of the fuel cell and its susceptibility to current ripple, it is required to interface dc-dc converter with high voltage gain and low current ripple between fuel cell and dc bus to satisfy the load demand [3]. Currently, several non-isolated dc-dc converter topologies with the above characteristics have been proposed, among which, output series interleaved boost converter (OS-IBC) is a promising selection [4]. However, building a real power converter testbench to evaluate the behavior of the newly designed converter and test the associated controllers is an expensive and risky step. Therefore, in order to reduce both cost and risks, applying the real time simulation technique in the early design and development stage of the power converters is an effective and economical alternative [5].

However, it is particular challenge to conduct the real-time simulation for the power electronic converters, because a very small simulation time step is required to capture the characteristics of the high-frequency switching event as accurate as possible [6]. In general, the typical switching frequencies of power converters are ranging from 10kHz to a few MHz, which means that the simulation time step is located at the nanosecond level by considering that the real time simulation time step should be tens of times smaller than the switching period [7].

In order to ensure that the power electronic model can be solved in nanosecond level time step in real time, several methodologies focused on two aspects have been intensively explored to accelerate the simulation. On the one hand, using the field-programmable gate array (FPGA) as the computational engine to achieve a fast solution benefiting from its excellent parallelism capability to simultaneously process a large amount of computing tasks in real time [7]-[8]; on the other hand, using several simplified behavior models, such as averaged model, associated discrete circuit model, binary resistor model and switching function model, to represent the nonlinear power switches, reducing the complexity of the model while retaining sufficient accuracy [9]. Among these switch models, the binary resistor model, which using a large conductance or a small conductance to model the switch on state or off state respectively, is especially suitable for the higher frequency power electronic converter, since it introduces no artificial oscillations and virtual power losses. However, the frequent changes of the switch status will lead to the heavier computational burden of matrix inversion in real time. One feasible solution is to precompute and store all the possibilities of the admittance matrix inverse for improving the computation efficiencies, but the more memory units are required [10]. Therefore, this binary resistor switch model is not suitable for the power electronic converter with the large number of power switches.

Apart from the electrical behavior of the power switches, modeling their thermal behavior in the real-time simulation is also very crucial since the reliability of the power devices depends strongly on the device thermal stress [11]. The devices junction temperature is determined by the device power losses and its transient thermal impedance. By using a constant thermal resistor–capacitor (RC) network to represent thermal impedance, the junction temperature can be estimated by feeding the thermal network with the time-varying power losses in real time. In general, the power losses can be classified as conduction loss and switching loss. The conduction loss can be straightforwardly computed according to the output characteristics of the power semiconductors. For the switching loss, different approaches can be used to obtain it. One direct approach is to generate the detailed switching transient waveforms by the device-level real time simulation, but it is time consuming [12]. Another way is to obtain the switching loss by fitting the loss curves from the device datasheet [13], which is computationally efficient but may

introduce the complicated mathematical formulae when the more arguments related to energy losses are involved. In addition, multi-dimensional lookup table (LUT) is also a feasible method to model the switching loss which stores appropriate number of energy loss samples and estimates the losses under arbitrary operating conditions by linear interpolation [14]. Based on this method, the fast estimation of switching loss can be achieved because only some simple math operations are involved in this process. Although the method has been normally applied in some commercial simulation software such as PLECS [15], it is considerably new in its implementation for power electronic converter real-time simulation.

This paper is focused on developing a LUT-based electro-thermal model of OS-IBC for FPGA-based real-time simulation. This developed electro-thermal model is composed of the electrical model, the power loss model based on LUT and the thermal model. The developed model is then designed and implemented in NI FlexRIO PXIe-7975R FPGA module equipped with a Kintex-7 XC7K70T FPGA, which allows achieving a 200ns real-time simulation time step. Moreover, the accuracy and the effectiveness of the electro-thermal model are validated by comparing with the results from PLECS software.

The rest of this paper is structured as follows. First, the LUT-based electro-thermal model of OS-IBC is elaborated in Section II. Next, the detailed hardware deployment on FPGA is illustrated in Section III, and then Section IV presents the FPGA-based simulation results and the verification by offline simulation on PLECS. At last, the conclusions are drawn in Section V.

II. LUT-BASED ELECTRO-THERMAL MODELING OF OS-IBC

Firstly, the used power devices in this paper are presented. The target power device is a 1200V/300A silicon carbide (SiC) chopper module (BSM300C12P3E301) consisting of SiC-UMOSFET and SiC-Schottky barrier diode (SBD) from ROHM [16]. It can provide more excellent switching characteristics and lower on-state voltage drop compared with the Si-based power devices [17]. More importantly, the reverse recovery loss generated by the SiC-SBD is almost negligible [18]. Therefore, based on the power module configuration, the developed LUT-based electro-thermal model, whose block diagram is depicted in Fig.1, contains three parts: (1) the electrical model for solving all the current through and voltage across the components; (2) the LUT-based power losses computation unit for estimating the conduction losses of the MOSFET and diode and the switching losses of the MOSFET; and (3) the thermal model for estimating the device junction temperature, which will feed back to power losses computation unit to affect the estimation of power losses at the next time step. It should be pointed that the influence of junction temperature on the performance of the electrical model is not considered here since the ideal switch model is used in this circuit.

A. Electrical model

Owing to the high voltage gain, the low current ripple and the low component stress, OS-IBC is a preferred interface between the fuel cell and the dc bus. The topology of OS-IBC

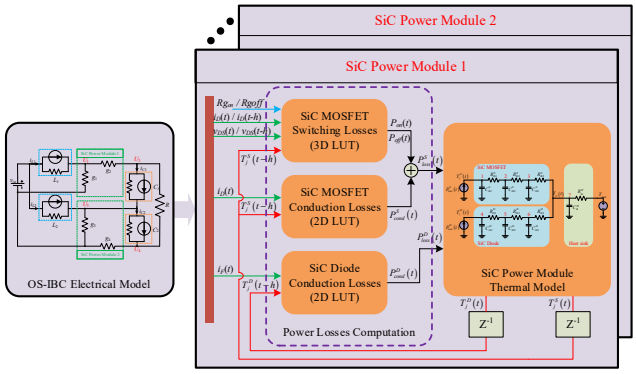


Fig.1. Block diagram of LUT-based electro-thermal model.

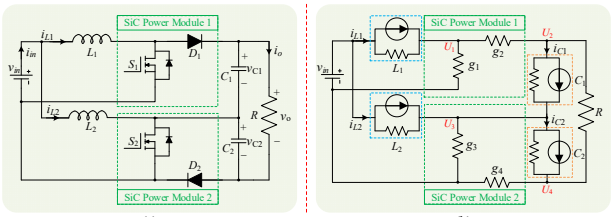


Fig.2. (a) OS-IBC topology; (b) The corresponding discrete time model.

is shown in Fig.2 (a), in which L_1 and L_2 are the inductors, C_1 and C_2 are the capacitors, R is the load, S_1 and S_2 are the SiC MOSFET, D_1 and D_2 are the SiC diodes, and v_{in} is the input voltage. Before modeling this converter using nodal analysis method, it is required to discretize all the elements.

The inductor and the capacitor can be equivalent to a constant conductance in parallel with a companion current source at current time t by using the backward Euler method with the given time step h, as expressed in (1),

$$\begin{cases} i_{L_i}(t) = g_{L_i} \cdot v_{L_i}(t) + i_{L_i}(t-h) \\ i_{C_i}(t) = g_{C_i} \cdot \left(v_{C_i}(t) - v_{C_i}(t-h)\right) \end{cases} \quad i = 1,2 \tag{1}$$

where $g_{Li}=h/L_i$ and $g_{Ci}=C_i/h$.

Additionally, the simple binary resistor model is employed to model the switch device as given in (2),

$$g_i(t) = \begin{cases} g_{on} & \text{on-state} \\ g_{off} & \text{off-state} \end{cases} \quad i = 1,2,3,4 \tag{2}$$

where g_i is denoted as the conductance.

As a result, the corresponding discrete-time model of OS-IBC is shown in Fig.2(b). Then, the nodal equations can be formed as (3),

$$Y(t) \cdot U(t) = I(t) \Rightarrow U(t) = Y^{-1}(t) \cdot I(t) \tag{3}$$

where $U(t)=[U_1 \;\; U_2 \;\; U_3 \;\; U_4]^T$ is the vector of the unknown nodal potentials. The nodal admittance matrix $Y(t)$ and the vector of current sources $I(t)$ are defined as (4) and (5).

$$Y(t) = \begin{bmatrix} g_{L_1}+g_1+g_2 & -g_2 & 0 & 0 \\ -g_2 & g+g_{C_1}+g_2 & -g_{C_1} & -g \\ 0 & -g_{C_1} & g_{C_1}+g_{L_2}+g_3+g_{C_2} & -g_{C_2} \\ 0 & -g & -g_{C_2} & g_{C_2}+g+g_{C_4} \end{bmatrix} \tag{4}$$

$$I(t) = \underbrace{\begin{bmatrix} 1 & 0 & 0 & 0 & g_{L_1} \\ 0 & 0 & g_{C_1} & 0 & 0 \\ 0 & 1 & -g_{C_1} & g_{C_2} & g_{L_2} \\ 0 & 0 & 0 & -g_{C_2} & 0 \end{bmatrix}}_{C(t)} \begin{bmatrix} \overbrace{\begin{bmatrix} i_{L_1}(t-h) \\ i_{L_2}(t-h) \\ v_{C_1}(t-h) \\ v_{C_2}(t-h) \end{bmatrix}}^{x(t-h)} \\ v_{in}(t) \end{bmatrix} \tag{5}$$

Obviously, the entries in the nodal admittance matrix Y will be varied with the switch states. Therefore, it is necessary to determine them according to the inductor current i_L, i_{L2} and the gate signal u_1, u_2 at the beginning of each time step. A simple state machine illustrated in Fig.3 is designed to identify the switch states. For the forced commutated switches such as MOSFET, their on/off status are controlled only by the gate signals u; while for the naturally commutated switches like diode, the direction of the inductor current i_L should also be accounted for. It is noteworthy that the switch state identifications of diode D_1 and D_2 are different because of the asymmetrical circuit structure.

Subsequently, the global state in (1) should be updated using the following equation for the next time step.

$$\underbrace{\begin{bmatrix} i_{L_1}(t) \\ i_{L_2}(t) \\ v_{C_1}(t) \\ v_{C_2}(t) \end{bmatrix}}_{x(t)} = \underbrace{\begin{bmatrix} 1 & 0 & 0 & 0 & g_{L_1} \\ 0 & 1 & 0 & 0 & g_{L_2} \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \end{bmatrix}}_{D(t)} \begin{bmatrix} x(t-h) \\ v_{in}(t) \end{bmatrix} + \underbrace{\begin{bmatrix} -g_{L_1} & 0 & 0 & 0 \\ 0 & 0 & -g_{L_2} & 0 \\ 0 & 1 & -1 & 0 \\ 0 & 0 & 1 & -1 \end{bmatrix}}_{E(t)} U(t) \tag{6}$$

In order to improve the computational efficiency, the final equation in a state-space form used to solve the electrical model can be derived by combining (3), (4), (5) and (6).

$$x(t) = \underbrace{\left(D(t) + E(t) \cdot Y^{-1}(t) \cdot C(t)\right)}_{A(t)} \cdot \left[x(t-h)\ v_{in}(t)\right]^T \tag{7}$$

Given that it is time consuming to calculate the coefficient matrix A in real time, a straightforward method is to compute offline all the possibilities (2^4) of the matrix A based on the permutations of switch states and store them in the specific memory unit. In fact, only 9 possible cases need to be stored for the OS-IBC by analyzing Fig.3.

At last, the drain source voltage v_{DS} and the drain current i_D in MOSFET, and the forward current i_F in diode will be computed for the later power losses estimation.

$$\begin{cases} v_{DS_1}(t) = v_{in}(t) - \left(i_{L_1}(t) - i_{L_1}(t-h)\right) \cdot g_{L_1}^{-1} \\ v_{DS_2}(t) = v_{in}(t) - \left(i_{L_2}(t) - i_{L_2}(t-h)\right) \cdot g_{L_1}^{-2} \\ i_{D_1}(t) = v_{DS_1}(t) \cdot g_1(t) \\ i_{D_2}(t) = v_{DS_2}(t) \cdot g_2(t) \\ i_{F_1}(t) = i_{L_1}(t) - i_{D_1}(t) \\ i_{F_2}(t) = i_{L_2}(t) - i_{D_2}(t) + i_{F_1}(t) \end{cases} \tag{8}$$

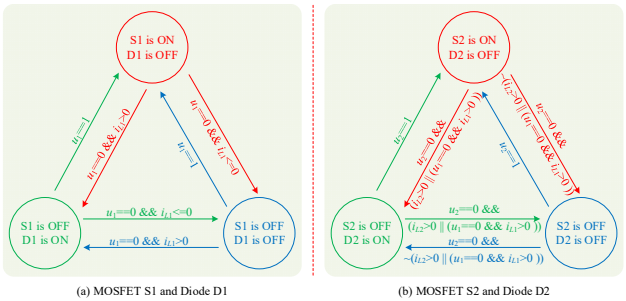
B. *Conduction loss computation*

Due to the non-ideal nature of the power semiconductors, they will produce the power losses, which can be distinguished by the conduction loss and the switching loss. The conduction loss at each time step can be directly calculated as the product of the current through the MOSFET or diode when it is in full conduction and the voltage across it, as shown in (9),

$$\begin{cases} P_{cond}^{S}(t) = v_{DS}(t) \cdot i_D(t) \\ P_{cond}^{D}(t) = v_F(t) \cdot i_F(t) \end{cases} \tag{9}$$

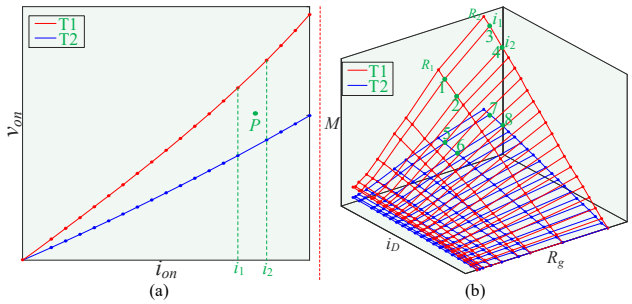
where P_{cond} represents the conduction losses, the superscript S and D represent the MOSFET and diode, respectively; and v_F is the forward voltage drop of the diode. It is noteworthy that the drain source voltage v_{DS} obtained from (8) can not be used for (9) due to the use of the ideal switch model.

Therefore, in this paper, a two-dimensional (2D) LUT is utilized to store a series of actual voltage drop under the different junction temperature T_j and conductive current i_D or i_F.



(a) MOSFET S1 and Diode D1 (b) MOSFET S2 and Diode D2

Fig.3. The state machine for the switch state identification



(a) (b)

Fig.4. The illustration of linear interpolation for (a) 2D LUT; (b) 3D LUT.

Note that the voltage drop dataset can be downloaded from the web page of manufacturers of the power semiconductor devices [16]. Since the sample points stored in LUT are limited, the bilinear interpolation is used to approximate the voltage drop for others operating conditions under the given operating range. Specifically, when the instantaneous junction temperature T_j lies within T_1 and T_2, and the instantaneous conductive current i_D or i_F lies within i_1 and i_2, the voltage drop at current time step t can be computed by (10) derived from Fig.4(a). The conduction losses under arbitrary instantaneous input values can then be obtained by substituting the estimated voltage drop into (9).

$$\begin{cases} v_{on}(T_1, i_{on}) = \dfrac{v_{on}^{LUT}(T_1, i_2) - v_{on}^{LUT}(T_1, i_1)}{i_2 - i_1}(i_{on} - i_1) + v_{on}^{LUT}(T_1, i_1) \\ v_{on}(T_2, i_{on}) = \dfrac{v_{on}^{LUT}(T_2, i_2) - v_{on}^{LUT}(T_2, i_1)}{i_2 - i_1}(i_{on} - i_1) + v_{on}^{LUT}(T_2, i_1) \\ v_{on}(T_j, i_{on}) = \dfrac{v_{on}(T_2, i_{on}) - v_{on}(T_1, i_{on})}{T_2 - T_1}(T_j - T_1) + v_{on}(T_1, i_{on}) \end{cases} \tag{10}$$

where i_{on} denotes as i_D or i_F, and v_{on} denotes as v_{DS} or v_F, and the superscript LUT represents that the values can be read from the LUT.

C. *Switching loss computation*

As for the switching energy loss produced in the switching transient including turn-on energy loss E_{on} and turn-off energy loss E_{off}, it is relatively more complicated to calculate than the conduction loss, because they depend on numerous factors, such as the drain current i_D, drain source voltage v_{DS}, junction temperature T_j and gate on-resistance Rg_{on} or gate off-resistance Rg_{off}. Considering that the switching power losses cannot be directly acquired based on the above electrical model, the following expression come from the thermal semiconductor models provided by ROHM will be used to compute the turn-on power loss P_{on} and turn-off power loss P_{off}.

$$\begin{cases} P_{on}(t) = \dfrac{E_{on}\left(T_j, R_{gon}, i_D^{post}\right)}{h \cdot v_{const}} \cdot v_{DS}^{pre} = M_{on} \cdot v_{DS}^{pre} \\ P_{off}(t) = \dfrac{E_{off}\left(T_j, R_{goff}, i_D^{pre}\right)}{h \cdot v_{const}} \cdot v_{DS}^{post} = M_{off} \cdot v_{DS}^{post} \end{cases} \tag{11}$$

where h represents one time step; v_{const} is a constant voltage; superscript pre and post are respectively an abbreviation for pre-switching and post-switching.

According to (11), it is required to create a three-dimensional (3D) LUT for storing lots of actual values of M_{on} and M_{off} under the various junction temperature T_j, gate resistance R_g and conductive current i_D. As in the case of conduction losses computation, for the arbitrary operating conditions at the given operating range, (for example, the instantaneous junction temperature T_j is in the interval T_1 and T_2, and the gate resistance R_g is in the interval R_1 and R_2, and the instantaneous conductive current i_D is in the interval i_1 and i_2), the instantaneous value $M(T_j,R_g,i_D)$ can be obtained by trilinear interpolation. The detailed implementation process is deduced as (12) with the help of Fig.4(b).

$$\begin{cases} M_{12}(T_1,R_1,i_D)=\dfrac{M^{LUT}(T_1,R_1,i_2)-M^{LUT}(T_1,R_1,i_1)}{i_2-i_1}(i_D-i_1)+M^{LUT}(T_1,R_1,i_1) \\ M_{34}(T_1,R_2,i_D)=\dfrac{M^{LUT}(T_1,R_2,i_2)-M^{LUT}(T_1,R_2,i_1)}{i_2-i_1}(i_D-i_1)+M^{LUT}(T_1,R_2,i_1) \\ M_{56}(T_2,R_1,i_D)=\dfrac{M^{LUT}(T_2,R_1,i_2)-M^{LUT}(T_2,R_1,i_1)}{i_2-i_1}(i_D-i_1)+M^{LUT}(T_2,R_1,i_1) \\ M_{78}(T_2,R_2,i_D)=\dfrac{M^{LUT}(T_2,R_2,i_2)-M^{LUT}(T_2,R_2,i_1)}{i_2-i_1}(i_D-i_1)+M^{LUT}(T_2,R_2,i_1) \\ M(T_1,R_g,i_D)=\dfrac{M_{34}(T_1,R_2,i_D)-M_{12}(T_1,R_1,i_D)}{R_2-R_1}(R_g-R_1)+M_{12}(T_1,R_1,i_D) \\ M(T_2,R_g,i_D)=\dfrac{M_{78}(T_2,R_2,i_D)-M_{56}(T_2,R_1,i_D)}{R_2-R_1}(R_g-R_1)+M_{56}(T_2,R_1,i_D) \\ M(T_j,R_g,i_D)=\dfrac{M(T_2,R_g,i_D)-M(T_1,R_g,i_D)}{T_2-T_1}(T_j-T_1)+M(T_1,R_g,i_D) \end{cases} \quad (12)$$

where R_g refers to Rg_{on} or Rg_{off}, and i_D refers to i_D^{pre} or i_D^{post}, and M refers to M_{on} or M_{off}. It should be mentioned that the datasets M^{LUT} stored in LUT can be collected by post processing the E_{on} and E_{off} provided by manufacturers using (11).

D. *Thermal model*

Due to the existence of thermal resistance and thermal capacity in the power semiconductor, the junction temperature will gradually rise to steady state when the heat induced by the power losses flows through them. To compute the variation of junction temperature, a typical thermal model composed of networks of resistors and capacitors, known as Cauer-model, is employed to imitate the transient thermal impedance, as shown in Fig.5. Then by applying the power losses P_{loss} as a current source injected to this network and applying the ambient temperature T_{amb} as a bias voltage source, the device temperature of each layer in the semiconductor structure can thus be accessed by the corresponding node voltage, such as the junction temperature T_j and the case temperature T_c. Meanwhile, a heat sink is merged after the node of T_c to withstand the rise of the junction temperature.

At last, employing backward Euler method with a time step h to discretize the thermal model, the temperature $T=[T_1 \cdots T_7]^T$ for each node at the current time t can be determined by (13),

$$T(t)=\underbrace{(I-h\cdot A_{th})^{-1}}_{F}T(t-h)+\underbrace{(I-h\cdot A_{th})^{-1}\cdot h\cdot B_{th}}_{G}\cdot\left[P_{loss}^{S}(t)\quad P_{loss}^{D}(t)\quad T_{amb}(t)\right]^T \quad (13)$$

where I is an identity matrix and P_{loss} is a total power loss for the MOSFET or diode. Coefficient matrices F and G are constant which can be precomputed and stored in memory unit.

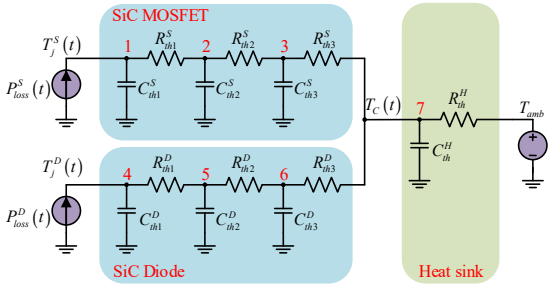


Fig.5. The Cauer thermal model for the SiC power module.

III. MODEL IMPLEMENTATION ON FPGA

In this paper, the developed LUT-based electro-thermal model of OS-IBC is implemented on Xilinx Kintex-7 XC7K410T FPGA, embedded in the National Instrument (NI) FlexRIO PXIe-7975R FPGA modules. The FPGA hardware is programmed by using a graphical programming approach in LABVIEW FPGA environment. Furthermore, with the help of LABVIEW IP builder tool, all the hardware can be synthesized into an IP block and executed under a single cycle timed loop (SCTL) structure with a specific clock by user, so that a strict time constraint can be met. In this design, a 40-bit word fixed-point numerical representation is adopted, and the clock of SCTL is set to 50MHz.

According to Fig.1, the overall diagram of the FPGA hardware implementation depicted in Fig.6 is constituted by three basic modules, including electrical model solver module 1, power losses computation module 2, and the junction temperature computation module 3. At the beginning of each time step, the switch states are recognized based on the state machine displayed in Fig.3, and the corresponding coefficient matrix A is thus selected in accordance with the combination of switch status and used to calculate the state variables of present time step. Then, the power devices' voltage and current can be obtained based on (8), which will be sent to module 2 for power losses computation. Before computing the switching losses, the turn-on and turn-off switching actions should be identified by comparing the gate signals of present time step with those of previous time step. Then, the corresponding pre-switching and post-switching values of the current flowing into the power module, and the gate resistance and the junction temperature are together used to read 8 sampled points from 3D LUT and thus the final value can be estimated by using trilinear interpolation. Similarly, the conduction loss of the MOSFET and the diode can also be calculated by combining the 2D LUT and the bilinear interpolation. It is worth noting that the reciprocal of interval (such as the interval i_1 and i_2 in Fig.4) are precomputed offline to avoid the use of division operation in the linear interpolation process. At last, the junction temperature of power module can be predicted based on (13) after injecting the obtained power losses to the thermal network. In addition, from eq. (7) and eq. (13), it can be seen that they are formulated as matrix-vector multiplication so that the computational latencies can be reduced remarkably by processing them in parallel. At the end of time step, the history items and the state variables are updated by shift registers and prepared for the computation of the next time step.

By using IP builder tool, all the above designed modules can be packaged into an IP core, which can reach 10 cycles initial interval and 9 cycles latency at 50MHz after configuring

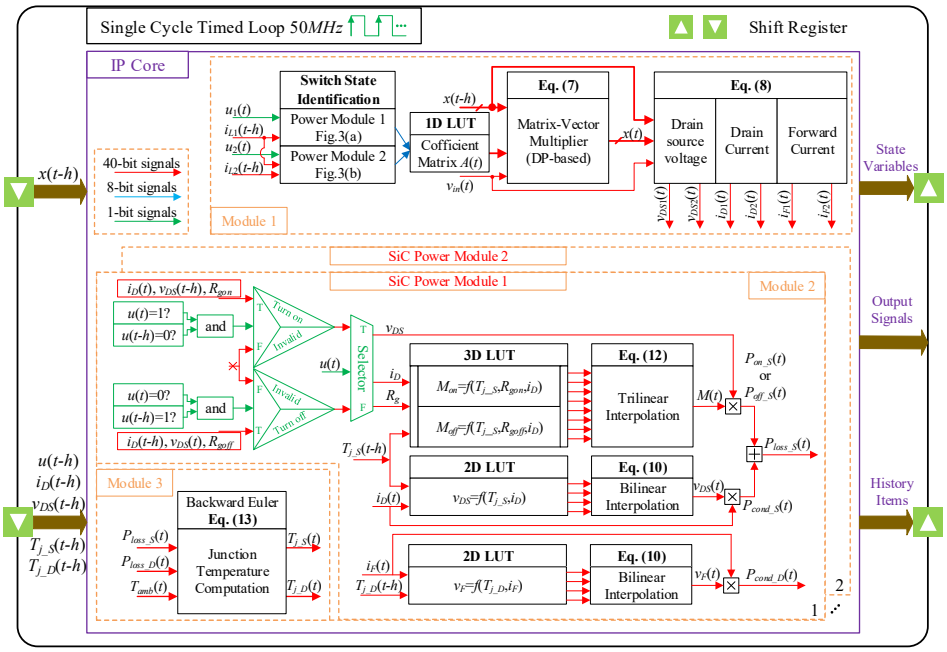


Fig.6. The overall diagram of the FPGA hardware design.

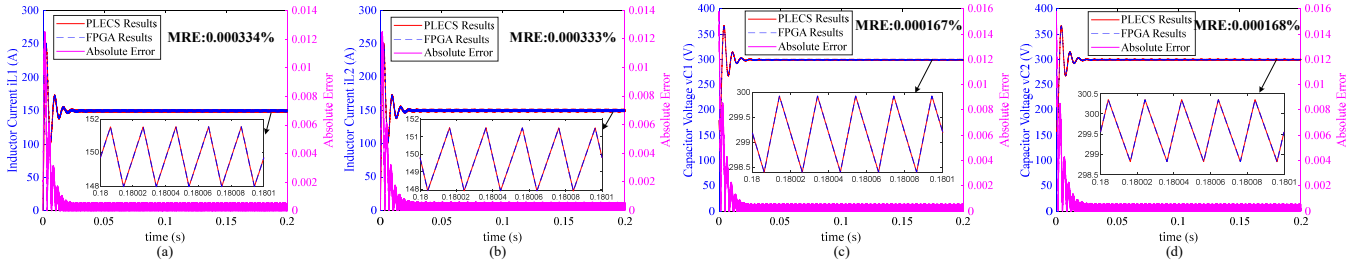


Fig.7. FPGA-based simulation results versus PLECS-based simulation results. (a) Inductor current i_{L1}; (b) Inductor current i_{L2}; (c) Capacitor voltage v_{C1}; (d) Capacitor voltage v_{C2}.

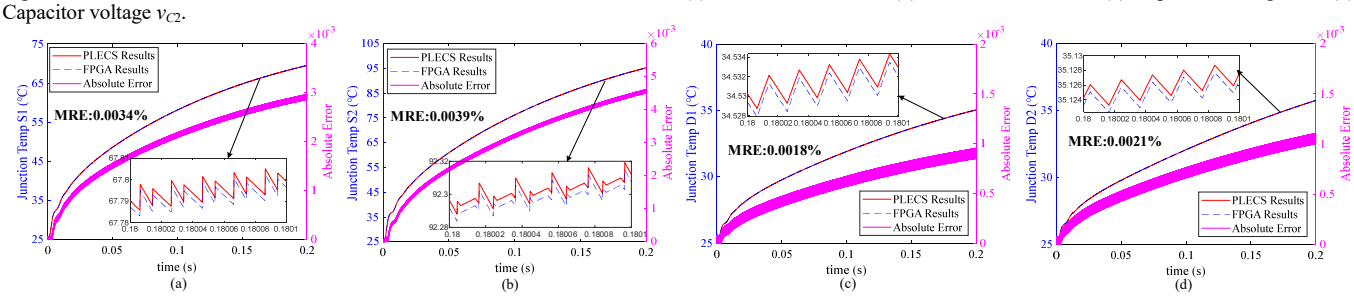


Fig.8. FPGA-based simulation results versus PLECS-based simulation results. (a) MOSFET S1 junction temperature; (b) MOSFET S2 junction temperature; (c) Diode D1 junction temperature; (d) Diode D2 junction temperature.

different optimization directives. The generated IP core is then settled into the SCTL with a 50MHz clock rate to execute and a valid output results can be obtained every 10 cycles, which means the model can be simulated with a 200ns time step in real time. Last, the code is compiled into bit-file and download into FPGA for real time simulation. Based on the compilation results, the timing performance is met without any violation and the final device utilization is listed in Table I.

TABLE I. DEVICE UTILIZATION ON XC7K410T FPGA

Device	Total	Used	Percentage
Total Slices	63550	23035	36.2%
Slice Registers	508400	51044	10.0%
Slice LUTs	254200	64895	25.5%
Block RAMs	795	121	15.2%
DSP48s	1540	430	27.9%

TABLE II. PARAMETERS OF ELECTRO-THERMAL MODEL OF OS-IBC

	Parameters	Values
Electrical Model	Input voltage v_{in}	120V
	Inductance L_1, L_2	400uH
	Capacitance C_1, C_2	470uF
	Load resistance R	10Ω
	Gate resistance R_g	R_{gon}:3.3Ω;R_{goff}:3.9Ω
	PWM frequency f_s	50KHz
	Conductance g_{on}/g_{off}	g_{on}=1000S;g_{off}=0S
Thermal Model	MOSFET S_1, S_2	R_{th}:[0.045, 0.041, 0.046]K/W C_{th}:[0.283,0.918,0.414]J/K
	Diode D_1, D_2	R_{th}:[0.045, 0.041, 0.046]K/W C_{th}:[0.283,0.918,0.414]J/K
	Heat sink H	R_{th}:[0.01]K/W C_{th}:[0.1] K/W
Solver	Simulation step h	200ns

IV. FPGA-BASED MODEL VALIDATION

In this section, the FPGA-based real-time simulation is conducted to evaluate the performance of the LUT-based electro-thermal model of OS-IBC. The simulation parameters of OS-IBC are summarized in Table II. In addition, for model comparison and validation purpose, the reference model with the same parameters is also built in PLECS 4.5.4 software. It should be mentioned that the OS-IBC is operating under the open-loop condition whose gate signals are shifted by 180° from each other, so that the error only comes from the model. The comparative simulation results of 0.2s simulation time can be obtained with 0.6 duty cycle and presented in Fig.7 and Fig.8.

Fig.7 shows the simulation results of the electrical model, including the inductor current i_{L1} and i_{L2}, and the capacitor voltage v_{C1} and v_{C2}. It can be clearly observed that the waveforms from FPGA-based simulation (blue line) are in good agreement with those from PLECS software (red line), which are also verified based on the corresponding absolute error (magenta line) between FPGA results and PLECS results.

In addition, the accuracy of the thermal model can be validated according to the simulation results of the power module junction temperature depicted in Fig.8. As it can be seen from the comparative results between FPGA results (blue line) and PLECS results (red line), all of them match well with only a very small error. Furthermore, it can be seen that the MOSFET S2 suffers the higher junction temperature than the MOSFET S1, since the asymmetrical circuit structure leads to the higher current stress on S2.

The mean relative errors (MRE) of the FPGA-based results over the PLECS results are also computed over 0.2 simulation time and displayed in the corresponding figure. Therefore, the effectiveness and the accuracy of the developed FPGA-based model can be validated from the above comparative results.

V. CONCLUSION

This paper presents a comprehensive design methodology of LUT-based electro-thermal real-time simulation model for output series interleaved boost converter. In this model, the LUT is not only used for avoiding solving the inverse matrix in real time, but also for quickly computing the power losses without the switching transient waveforms. In addition, the developed model can be simulated in FPGA-based real-time simulation platform with a 200ns time step, and the FPGA-based results showcase an excellent agreement with the results from PLECS software. Therefore, with the LUT-based electro-thermal model, we can quickly acquire an accurate thermal response of the power device, which can be used to optimize the parameters of power electronic systems and the heat dissipation system for the safe operation of power semiconductor devices. Unfortunately, due to the use of the ideal switch model, the effects of junction temperature on the electrical model are not considered, which will be explored in the future.

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