Integration of a CMOS LSI Chiplet into Micro Flexible Devices for Remote Electrostatic Actuation

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***Abstract*— In this paper, we proposed an integration method of a mm-scale high voltage (HV) driver and electrostatic actuators on a Parylene-C flexible substrate. With our unique three-layer metal structure (Cr/Au/Cr), we have demonstrated the contamination-less integration of an HV driver made of deep trench separated series silicon P-N junctions, bonded on the gold electrodes of the actuator. This technique enables CMOS LSI chips to directly be integrated with flexible electronics. Thus, novel applications of flexible electronics in various fields will be developed with the enhanced ability of signal processing, communications, and power delivery by CMOS LSI.**

Keywords—flexible electrode, LSI, electrostatic actuator, micro assembly

I. Introduction

Flexible electronics has attracted attention in a wide range of application fields such as biomedicine [1], wearable devices [2], and micro assembly [3] (Fig. 1). In real-field applications, such as large-area sensors and displays, large scale integrated circuits (LSI) are mandatory for signal processing, communications, and power delivery. They must be prepared in addition to the components of flexible electronics. To aim for a compact device, a direct combination of the flexible electronic device and an LSI chip was proposed [4]. Flexible integrated sensor arrays (FISA) and commercial packaged LSI chips on a flexible printed circuit board were electrically connected. However, the rigid package is not preferable to flexible electronics, and the large footprint of packages hinders the miniaturization of devices. It is therefore essential to embed LSIs directly into the flexible substrate. Organic transistors and thin film transistors have been investigated as a technology that can be fabricated directly on a flexible substrate. However, their carrier mobility is by more than two orders of magnitude as low as that of silicon. This low mobility strictly limits the performance of the device.

In this paper we propose the complementary metal-oxide-semiconductor (CMOS) compatible direct integration of silicon large scale integration (LSI) into flexible substrate. The flexible substrate that enclose the Si dice and wires eliminates the rigid and space-consuming package.

II. Design

Among the various application fields, this study focuses on the application to the micro assembly. Micro self-reconfigurable modular robots (SMR) have been prevented from miniaturizing their unit robot due to the difficulty of installation and wiring of LSI and actuators. If the LSI and actuators are integrated into a flexible device, the unit robot can be assembled only by wrapping a 3D-printed shell with

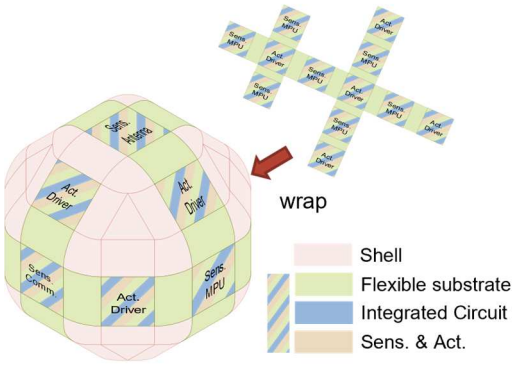


Fig. 1. Concept of micro assembly using flexible electronics.

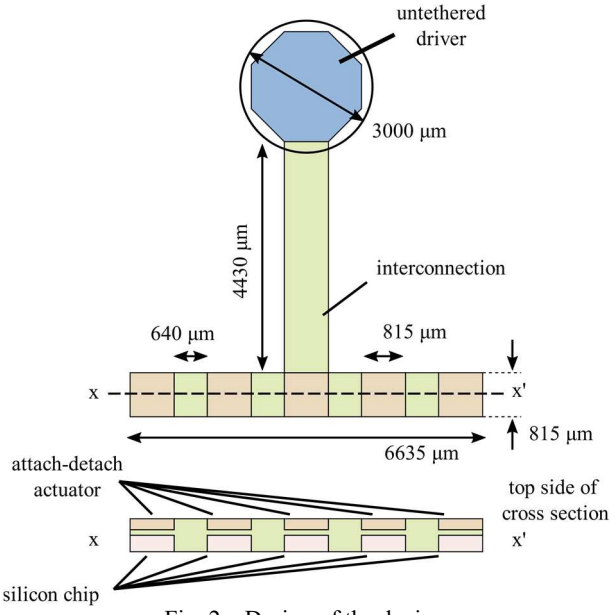


Fig. 2. Design of the device.

the flexible device. In this study, we designed the integration of a remote-controllable, energy-independent driver and electrostatically-actuated detachable connectors into the flexible substrate.

The shell of the unit robot has a quasi-spherical shape, which was optimized for rotation and connection, with a diameter of approximately 3 mm [5]. The device configuration determined from the shell design is shown in Fig. 2. At the top, the octagonal part painted in blue is dedicated to the driver. The driver is placed inside the shell and operates by the illumination of optical signals. On the other hand, the brown parts, to be flat when the device is assembled, are dedicated to the electrostatic connectors. Each connector, a pair of interdigitated Au electrodes, is located on the opposite side to the Si chip that foresees a future use (colored in pink). When a voltage is applied between the electrodes, an electrostatic force is generated that attracts an adjacent conductive body. The surface of the electrodes is covered with an insulation layer made of Parylene-C, which also works as a part of a flexible substrate. Behind the connector is SU-8 epoxy polymer as an adhesive between the Si chip and the flexible substrate. The dimension of each connector is 815 × 815 µm^2. The thickness of the insulation layer on the side of the connectors is 250 nm. It was suggested in our previous work that 250 nm is thin enough to generate an attractive force that sustains a unit robot itself, weighing approximately 40 mg, when the actuators were driven at 90 V. In contrast, the Parylene-C film for encapsulating Si chips on the opposite side is 10 µm thick.

III. Simulation of Attraction Force

The Si substrate beneath the Au electrode in our design can weaken the attraction force of the actuators. We simulated the output force using COMSOL Multiphysics to estimate the effect of the Si chips. In simulations, the gap between the surface of the actuators and the counter electrode of the other unit robot was set to be 2.2 µm as suggested in [3]. And other configurations were identical to that described in the previous section except for the thickness of SU-8 that separates the electrode and the Si chip.

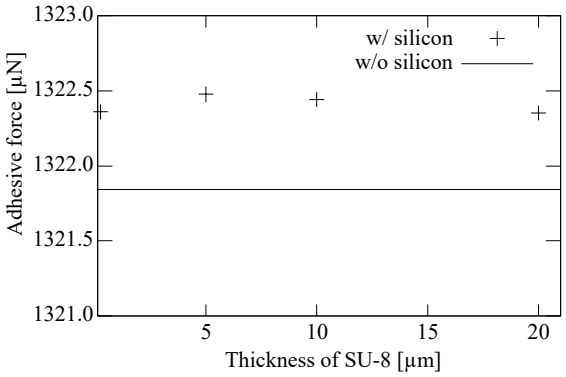


Fig. 3. Simulation result of the attraction force.

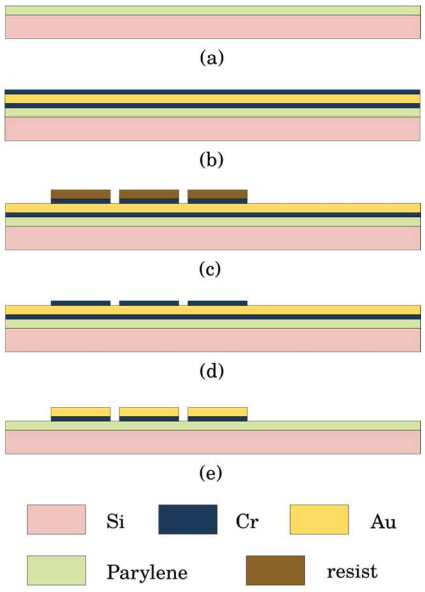


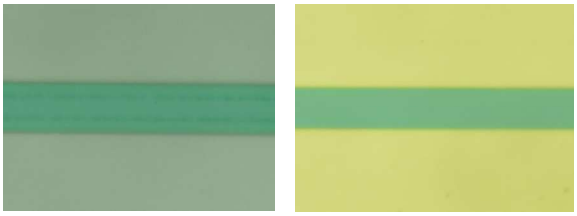
Fig. 4. Fabrication process of the connectors

Figure 3 shows the dependence of attraction force on the thickness of SU-8. The solid line is the calculated force without the Si chip. The result is almost constant at 1322.5 µN independently of the thickness of SU-8. Although the force was enhanced by the existence of the Si chip due to the edge effect, it is negligible since the deviation was less than 0.05% of the total value. Therefore, the thickness of SU-8 was determined to be 10 µm, with which CMOS Si chips can be integrated beneath the electrostatic actuators without any effects on the attracting force of the actuators.

IV. Fabrication Process

A. Electrostatically actuated detachable connectors

To fabricate the device, we composed the fabrication process with three phases: The electrostatic connectors on a flexible substrate, the driver, and their integration. First, we describe the process for the electrostatic actuators shown in Fig. 4. As mentioned above, the insulation layer of the electrostatic actuators must be thinner than 250 nm. Our fabrication process presented previously was not applicable for such a thin insulation layer device because delamination of Parylene-C film from handling substrate was caused in Ti adhesive layer etching step by soaking bubbles of ammonia-peroxide water mixture (APM) into breaks and pinholes of



(a) (b)

Fig. 5. Electrodes (a) before and (b) after Cr etching.

the film. Thus, we modified the process so as not to use APM. First, 250-nm thick Parylene-C was deposited on a 1-µm-thick thermal oxidized silicon chip after APM cleaning and dehydration. Next, 10-nm-Cr/100-nm-Au/10-nm-Cr was sputtered. The process of electrode patterning was composed of 5 steps. The first two steps were photolithography and chromium etching of the top layer by Cr etchant with a resist mask. After the top Cr layer etching, resist was removed by O_2 plasma ashing at the third step. At the continuing step, Au was etched by iodine-based etchant with the patterned top Cr layer as a mask. Finally, chromium on the surface, both in the first and the third layer, was etched by Cr etchant. The top layer of chromium not only improves adhesion of resist in lithography but also lift-off residue after electrode patterning (Fig. 5). Electrode patterning could be followed by pealing from handling substrate for completely passive devices or by integration of the driver described below for active devices.

The attraction force of 250-nm-thick electrostatic actuators was measured in an identical setup to [3] and it was 90.7 mgf which was enough large as mentioned above.

B. Photovoltaic cells and phototransistors

We adopted the deep trench isolated PV cells and PTs reported by Mori *et al.* [6]. Charge and discharge are remotely controllable by the color of light due to the built-in color-selective phototransistor. In addition, it outputs high output voltage, together making it suitable for the unit robots. In this paper, the number of PV cells connected in series is 192 and that of PTs is 2, considering the trade-off among area, current carrying capability, and output voltage. In addition to the original PV cells and PTs, the isolation trench was filled with Parylene-C for passivation and the substrate was thinned to 100 µm before deep reactive ion etching of the trench. As a whole, the driver is on with a red light and off with a green light.

I-V characteristics of the PV cells and the PTs fabricated were measured with a semiconductor parameter analyzer limiting currents to 1 µA. The light source is red LEDs and a green laser. Figure 6 shows the I-V characteristics of PV cells under red LED illumination and in the dark. Their short current, open voltage, and maximum output power are -260 nA, 98 V, and 20.0 µW respectively. On the other hand, Fig. 7(a) shows those of PTs in three conditions of illumination. First, in the dark current flow is zero ampere under the breakdown voltage around 96 V. Second is under red LED illumination. In this measurement, the number of green cellophane films as a color filter on PTs varied from one to three. When three films were covered with PTs, current flow at 94 V was suppressed under the output current of PVs at 97 V as shown in Fig. 7(b). Therefore, the driver can drive the

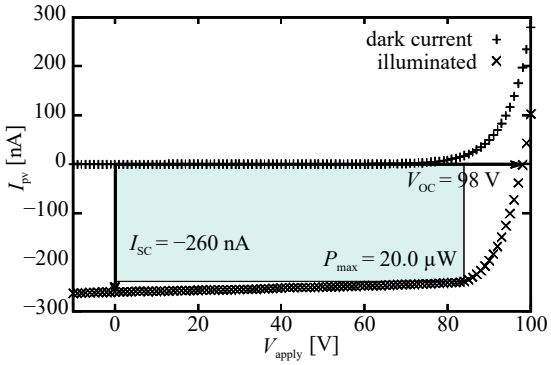


Fig. 6. I-V characteristic of PV cells.

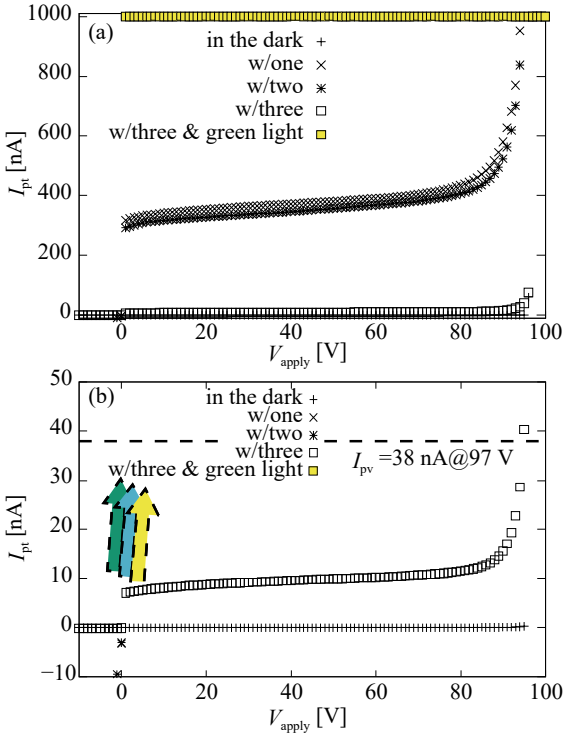


Fig. 7. I-V characteristics of PTs. (a) overview. (b) enlarged.

actuators at 94 V. Under the third condition that PTs were illuminated by LEDs and laser, the value of the current stacked at the upper limit. Consequently, our driver can switch the output force from approximately 90 mgf to 0 mgf by exposing it to a green laser under red LEDs illumination.

C. Integration of the actuators and the driver

There are two options for the integration of CMOS chips. One is the die integration and the other is the chiplet integration. Chiplet integration is dicing die into chiplets, small chips, first and bonding them separately to each face of flexible substrates. In contrast, die integration is bonding a die to a flexible substrate and removing parts other than the faces. We have concluded that the chiplet integration approach is simpler and more reliable for our multi-layer structured LSI integration. Moreover, the feature that chiplet integration can be adaptable for chiplets fabricated in various technologies on one flexible board, such as Si CMOS, III-V semiconductor, and MEMS, is suitable for components of the programmable matter.

The process flow of the integration is shown in Fig. 8. First, SU-8 epoxy polymer was spin-coated and patterned as adhesive on the flexible substrate with electrostatic actuators

and wire. Next, the driver chiplet was flip-chip bonded to the

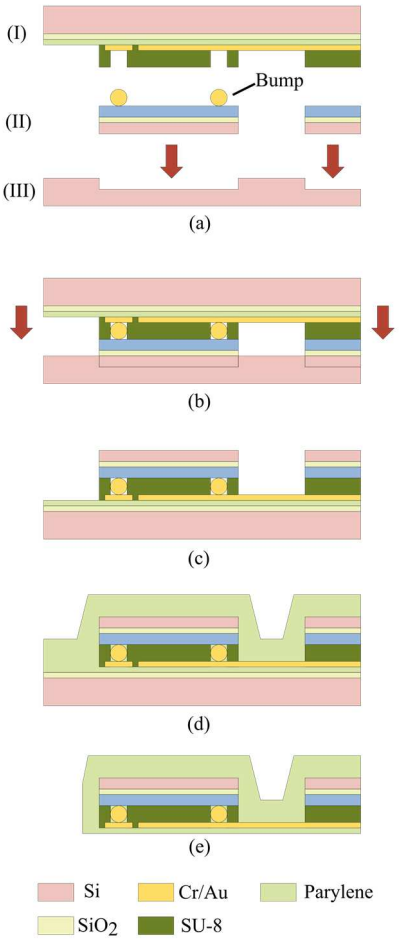


Fig. 8. Integration process.

substrate at 200°C. 10-µm-thick Parylene-C was deposited and was formed to be the outline of the device. Finally, the device was delaminated from handling substrate. Dipping into HF could assist it if the device was sticking strongly to the substrate.

V. Results and Discussions

The fabricated device is shown in Fig. 9. The silicon chiplets were integrated on the flexible substrate. Although in this study only the driver was implemented, other circuits, such as processors and transceivers, can be implemented on the bare silicon chips because of CMOS compatibility of our process. Moreover, chiplet integration can integrate chips in various technologies. for example, a III-V semiconductor chip for an optical sensor, a MEMS chip for a gyro sensor, and a CMOS chip for a processing unit.

Regarding electrode patterning, the Cr/Au/Cr structure is a key point for a clean electrode surface. Without the top layer of chromium, resist was stripped after Au or Cr etching. However, at this time we could not apply O_2 plasma cleaning, which was necessary for removing the resist after Au etching since it also damaged the Parylene-C layer. On the contrary, with the top layer of chromium, we stripped the resist before Au etching. O_2 plasma cleaning at this time was acceptable as 100-nm thick Au protected the Parylene-C layer from plasma. In addition, the resist that was not removed by the O_2 plasma was lifted-off at the fifth step of the electrode patterning.

VI. Conclusion

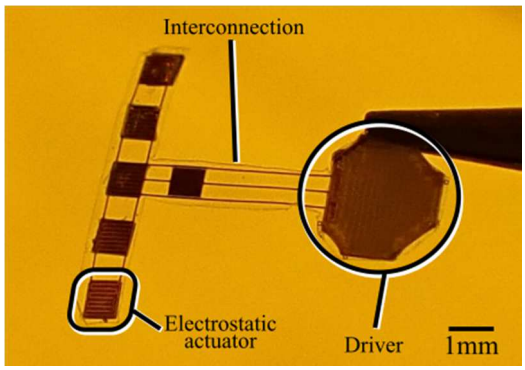


Fig. 9. Fabricated device.

We have realized the reliable integration method of Si CMOS LSI chips to a flexible substrate. The method was applied to fabricate the flexible device that integrated electrostatic attach-detachable connectors and their driver. This integration technique can develop the novel application of flexible electronics in various fields by enhancing the ability of signal processing, communications, and power delivery.

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