

Characterization of a surface electrode Paul trap for frequency metrology

J. Madunic, M. Abdel Hafiz, Y. Kersalé and C. Lacroûte

FEMTO-ST Institute, univ. Bourgogne Franche-Comté, CNRS, SUPERMICROTECH-ENSM, 26 rue de l'Épitaphe, 25000 Besançon, France

clement.lacroute@femto-st.fr

Summary—We report on the progress on a single-ion optical clock that is being developed at the FEMTO-ST institute. Our objective is to reach a fractional frequency stability of the order of 10^{-14} at one second for a total volume well below 500 L. The experimental setup is based on a surface electrode single-ion trap. A new trapping chip was designed and produced at the local cleanroom facility, using deep reactive-ion etching (DRIE) on a silicon on insulator- (SOI) wafer. Paul traps require a source of highly-stable and low noise voltage in the radio-frequency (RF) domain. A resonator of our own design has been used to supply high voltage to the trap. We have developed and implemented techniques for 3D micromotion reduction in order to minimize the 2nd order Doppler shift. Indeed, for Yb^+ optical spectroscopy, second order Doppler shift and Stark shift due to the ac fields can contribute significantly to the uncertainty budget. We will present the latest results of the trap characterization, which should include lifetime and heating rate measurements of the trap.

Keywords—atomic clock; single-ion trapping, heating rates, micro-motion reduction

I. INTRODUCTION

Optical frequency standards are the most accurate instruments nowadays. Optical clocks have achieved outstanding accuracies at the 10^{-18} level or below [1, 2] surpassing the best cesium clocks that currently define the time unit. For that reason, optical clocks are excellent candidates for applications in many fields of science. A growing number of laboratories around the world are developing transportable optical clocks [3] for various applications such as TF metrology, geodesy, fundamental physics, deep-space navigation and optical clocks networks.

All optical clocks work on the same basic principle. The operational cycle of an optical frequency standard consists of three steps: cooling and state preparation, interrogation, and detection and signal processing. We are developing a transportable optical clock of a total volume well below 500 L. We chose to work with a single, trapped $^{171}\text{Yb}^+$ ion on the quadrupole transition at 435.5 nm [4] and a planar Paul trap [5]. We implemented a simple 2D geometry and tested it as a prototype trap first. In this abstract, we present a new, custom micro-fabricated trap shown in Fig. 1, aiming in improvement of the ion lifetime and reduction of ion heating from the trap chip.

II. METHODS/RESULTS

We have developed a single-ion trap based on the 5-wire geometry [6]. The chip has 19 DC electrodes and a single RF electrode that is divided in half by the central DC electrode. The RF electrode lateral dimensions approximately are $600 \cdot 8000 \mu\text{m}^2$ and $1200 \cdot 8000 \mu\text{m}^2$. We used commercial, ultra-high vacuum (UHV) - compatible chip carrier. The electrodes are etched on doped silicon with a $20 \mu\text{m}$ distance and $200 \mu\text{m}$ of depth. This geometry suppresses the excess micromotion caused by possible dephasing of RF voltages. The vacuum chamber is described in [7].

We have also developed a custom resonant RF circuit for maximizing RF trapping voltages and quality factor for optimal trapping and electric field noise filtering. With our resonant RF circuit, we measured a quality factor of 100 for the resonance and a magnification factor of 10 for the voltage across the trap. Tests were performed under ultra-high vacuum using a testing chip, enabling breakdown voltages measurements as well.

We will present our RF circuit design and test results as well as our latest results on the new trap characterization, including the ion life time, micromotion reduction, and heating rate.

REFERENCES

- [1] Huntemann *et al.*, Phys. Rev. Lett. **116**, 10.1103 (2016).
- [2] Brewer *et al.*, Phys. Rev. Lett. **123**, 033201 (2019).
- [3] Cao *et al.*, Appl. Phys. B **123**, 10.1007 (2017).
- [4] Tamm *et al.*, Phys. Rev. A **61**, 053405 (2000).
- [5] Seidelin *et al.*, Phys. Rev. Lett. **96**, 253003 (2006).
- [6] Chiaverini *et al.*, Quantum Inf. Comput., **vol. 5**, 10.48550 (2005)
- [7] Delehay *et al.*, J. Mod. Opt. **65**, 10.1080/09500340 (2018).

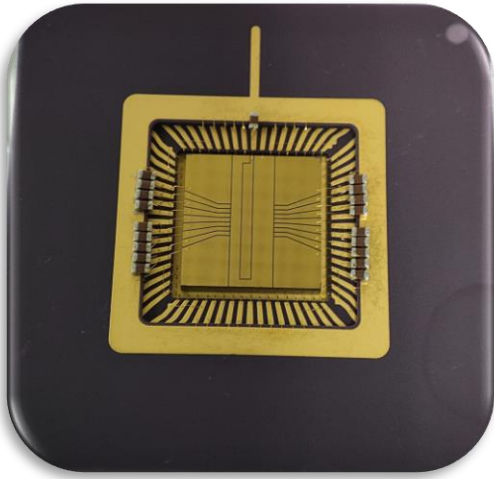


Fig.1. **Photograph of the planar ion trap.** The central part is a 5 wire surface electrode trap that has been produced at the local cleanroom facility, using deep reactive-ion etching (DRIE) on a silicon on insulator (SOI) wafer. The trap is embedded in a commercial, UHV compatible chip carrier. One can also see filter capacitors that prevent RF leakage to the DC electrodes.