L'électronique pour le calcul

Projet ciblé BEP

Towards An Algebraic Decomposition Of 3D Photonic Waveguide Circuits for Opto-Electronic Neuromorphic Chips

Jacob Puhalo-Smith[1], Damien Querlioz[2], Elisa Vianello[3], Jean-Michel Portal[4], Daniel Brunner[1]

[1] FEMTO-ST Institute/Optics Department, CNRS & University Franche-Comté, 15B avenue des Montboucons, 25030 Besançon Cedex, France.

[2] Université Paris-Saclay, CNRS, Centre de Nanosciences et de Nanotechnologies, Palaiseau, France.

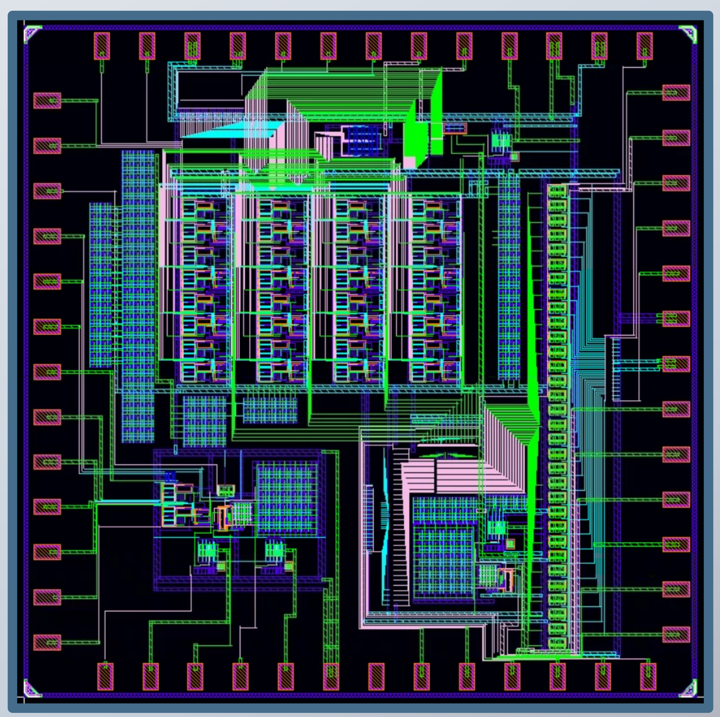
[3] Université Grenoble Alpes, CEA, LETI, Grenoble, France.

[4] Aix-Marseille Université, CNRS, Institut Matériaux Microélectronique Nanosciences de Provence, Marseille, France.

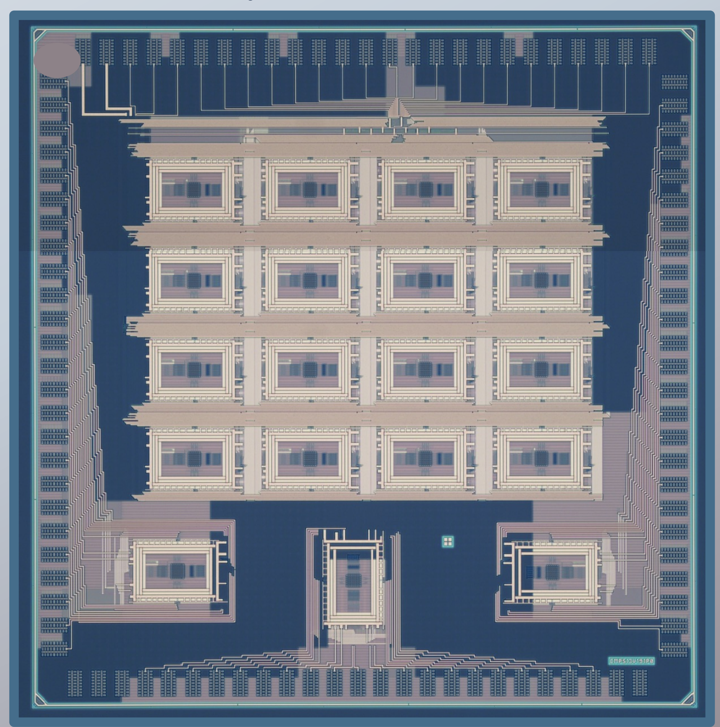
Abstract

Connecting several inputs to several outputs is a fundamental operation of computing. Implementing these connections and operations on *traditional* electronic architectures can quickly become computationally, ecologically and financially consuming. One novel approach to overcome these constraints is combine state-of-the-art electronics with photonics to design in-memory opto-electronic chips. Here, an outline of how we can design arbitrary circuits of 3D printed polymer waveguide interconnects, which will be integrate with neuromorphic electronic chips.

Opto-Electronic Neuromorphic Chips



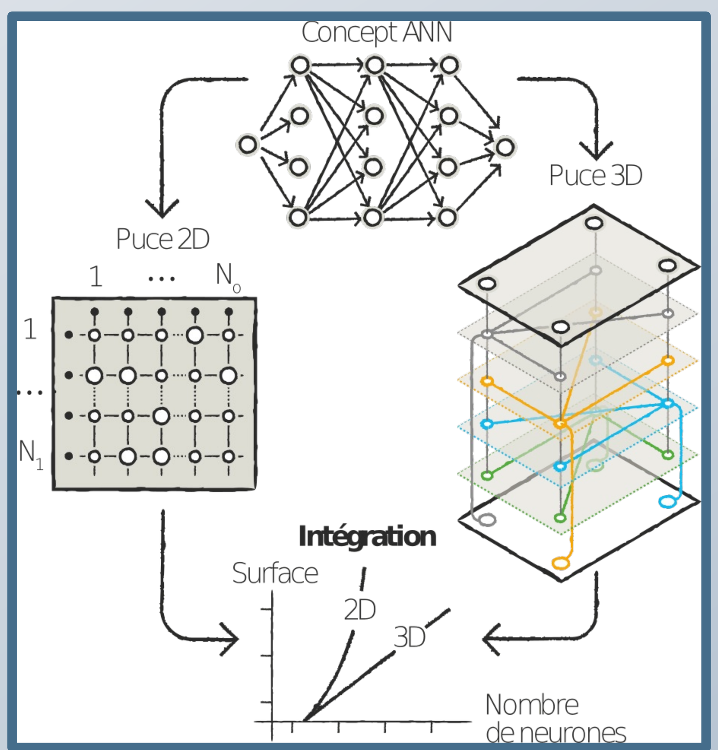
Design of hybrid Photodiode – RRAM chip on which we 3D waveguides will be fabricated.



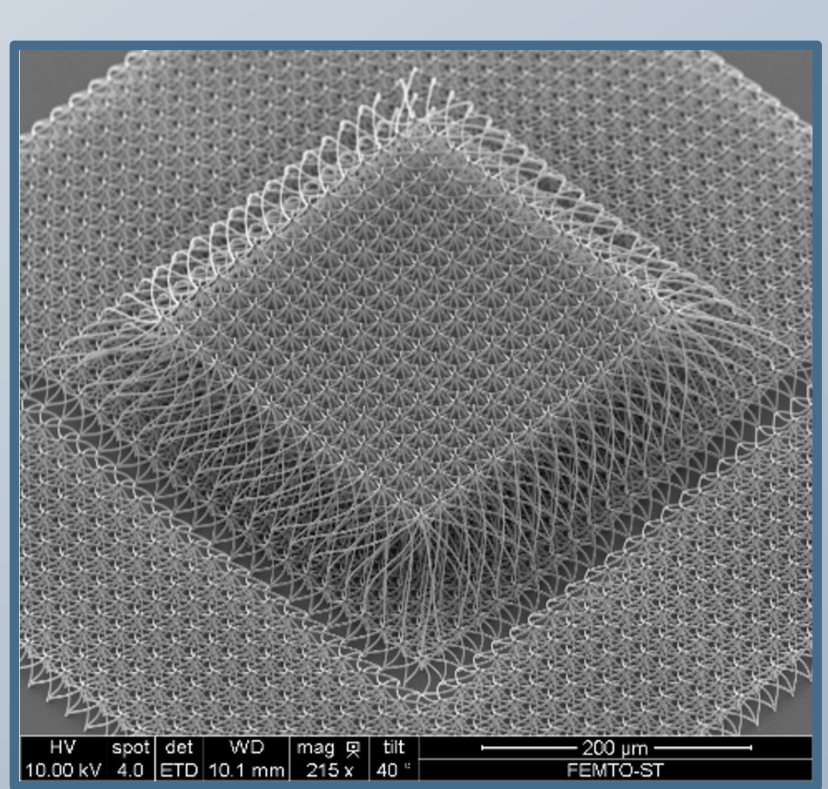
Memristor-based chip used for in-memory computing [1].

Why 3D?

In order to be comparable to current state-the-art *conventional* electronics, neuromorphic chips must have a comparable size. In 2D, the footprint (area) is $A \propto (N_I|N_O)^2$ while in 3D, $A \propto N_I|N_O$.



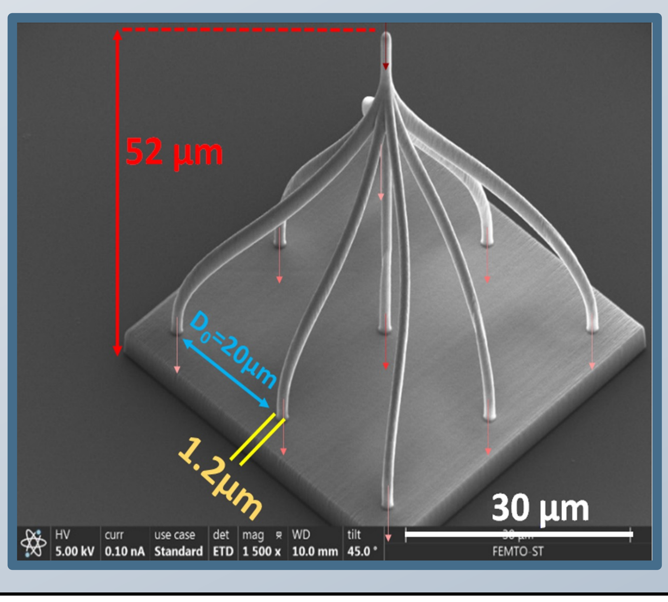
Scaling of 2D and 3D interconnects [2]

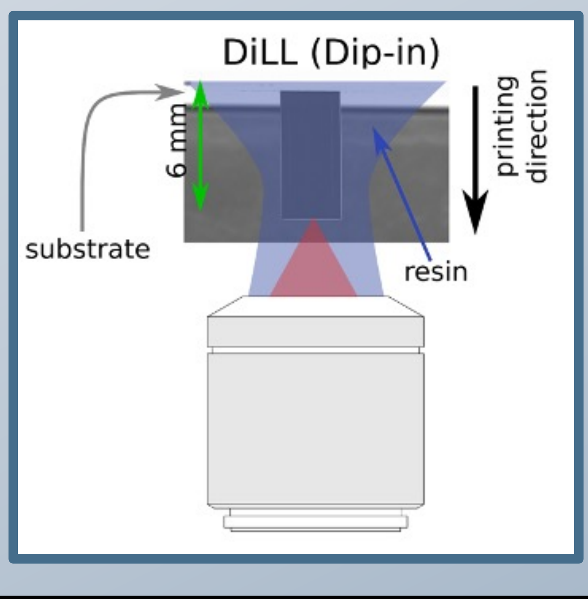


SEM Image of large array of 1x81 *interconnects* [3]

Fabrication

The waveguides are 3D printed via One and/or Two Photon Polymerization using commercially available hardware. The resolution is $\sim 0.5 \mu m$ while optical losses are $\sim 1 dBmm^{-1}$.





Left: SEM image of single 1x9 *splitter waveguide* [4].

Right: Schematic of printing 3D printing process via 2 Photon Polymerisation [4]

3D Circuit Design Procedure

Interconnect routing problems in 3D is an NP-complete [5], [6] and thus is difficult to achieve. Given an array of optical inputs $\boldsymbol{U}_0$, the output array $\boldsymbol{Y}_F = \boldsymbol{M} \cdot \boldsymbol{U}_0$.

$$\boldsymbol{U}_{L_0} = \begin{pmatrix} u_{00} & & \cdots & & u_{0N_{L_0}} \\ & u_{i-1j-1} & u_{i-1j} & u_{i-1j+1} & \\ \vdots & u_{i-1j+1} & u_{ij} & u_{ij+1} & \vdots \\ & u_{i+1j-1} & u_{i+1j+1} & u_{i-1j+1} & \\ u_{N_{L_0}0} & & \cdots & & u_{N_{L_0}N_{L_0}} \end{pmatrix} \quad \boldsymbol{M} = \begin{pmatrix} \ddots & \vdots & & \vdots & ⋰ \\ \cdots & m_{i-1,j-1} & m_{i-1,j} & m_{i-1,j+1} & \cdots \\ \cdots & m_{i,j-1} & m_{i,j} & m_{i,j+1} & \cdots \\ \cdots & m_{i+1,j-1} & m_{i+1,j} & m_{i+1,j+1} & \cdots \\ ⋰ & \vdots & & \vdots & \ddots \end{pmatrix}$$

Using the waveguide interconnects with a low branching *(e.g. 1→4)*, we outline a algebraic procedure for decomposing $\boldsymbol{M}$ to allow for easy design of the circuits. This procedure involves two steps;

1. Branching Step – Determines how each input port is split in to a number of branches with a power ratio.

$$\boldsymbol{Z}_0 = \boldsymbol{U}_0 \otimes \boldsymbol{R}_0 \in \mathbb{R}^{N_{L_1} \times N_{L_1}}$$

where $\boldsymbol{R}$ is the is block matrix whose elements define the splitting ratio of each individual input port,

$$\boldsymbol{R}_0 = \begin{pmatrix} \boldsymbol{r}_{00} & \cdots & \boldsymbol{r}_{0N_{L_0}} \\ \vdots & \ddots & \vdots \\ \boldsymbol{r}_{N_{L_0}0} & \cdots & \boldsymbol{r}_{N_{L_0}N_{L_0}} \end{pmatrix}, \boldsymbol{r}_{ij} = \begin{pmatrix} r_{00}^{(ij)} & \cdots & r_{0N_{b_0}}^{(ij)} \\ \vdots & \ddots & \vdots \\ r_{N_{b_0}0}^{(ij)} & \cdots & r_{N_{b_0}N_{b_0}}^{(ij)} \end{pmatrix} \in \mathbb{R}^{N_{b_0} \times N_{b_0}}$$

N_{b_0} is even and corresponds to the largest branching ratio of the local splitter.

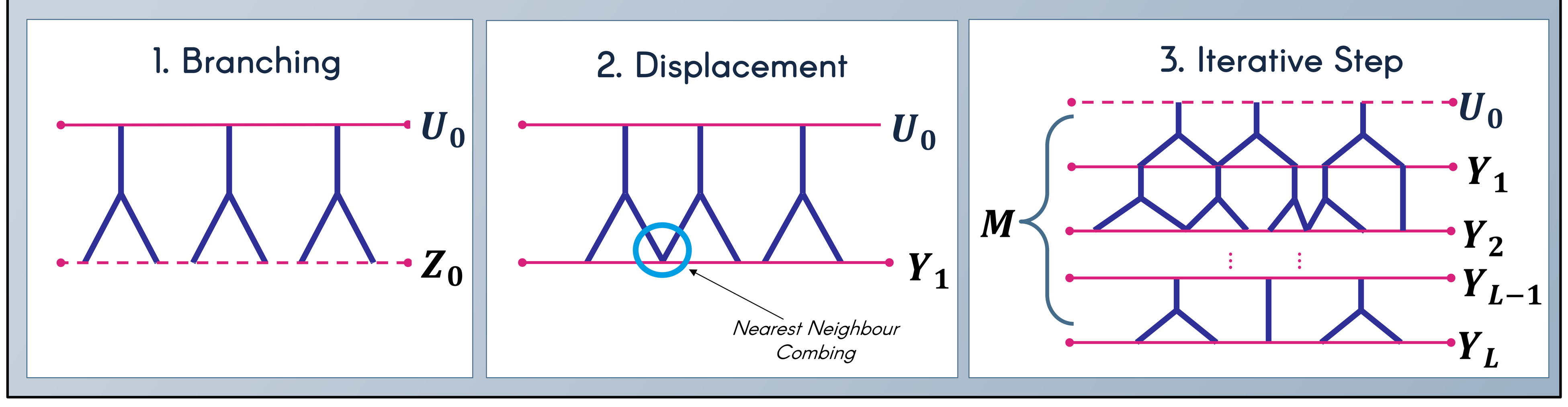
2. Displacement Step – Accounts for combing and displacement of the output ports in the new layer. This is achieved by considering the single-entry matrices that make up $\widetilde{\boldsymbol{Z}}_{L_0}^{(ij)} = \boldsymbol{Z}_{L_0} \odot \boldsymbol{E}_{ij}$. Here, '$\odot$' is the Hadamard Product and $\boldsymbol{E}_{ij}$ whose only non-zero value is element (i, j). Then calculating,

$$\boldsymbol{Y}_1 = \sum_{(i,j)} \boldsymbol{X}_{0\updownarrow}^{(ij)} \widetilde{\boldsymbol{Z}}_0^{(ij)} \boldsymbol{X}_{0\leftrightarrow}^{(ij)}$$

where $\boldsymbol{X}_{0\updownarrow}^{(ij)}$ ($\boldsymbol{X}_{0\leftrightarrow}^{(ij)}$) is sparse matrix whose only non-zero elements are along row (column) at which we wish to displace $z_0^{(ij)}$. Given the nearest neighbour constrain, we are therefore our choices $\boldsymbol{X}_{0\updownarrow}^{(ij)}$ and $\boldsymbol{X}_{0\leftrightarrow}^{(ij)}$ are restricted.

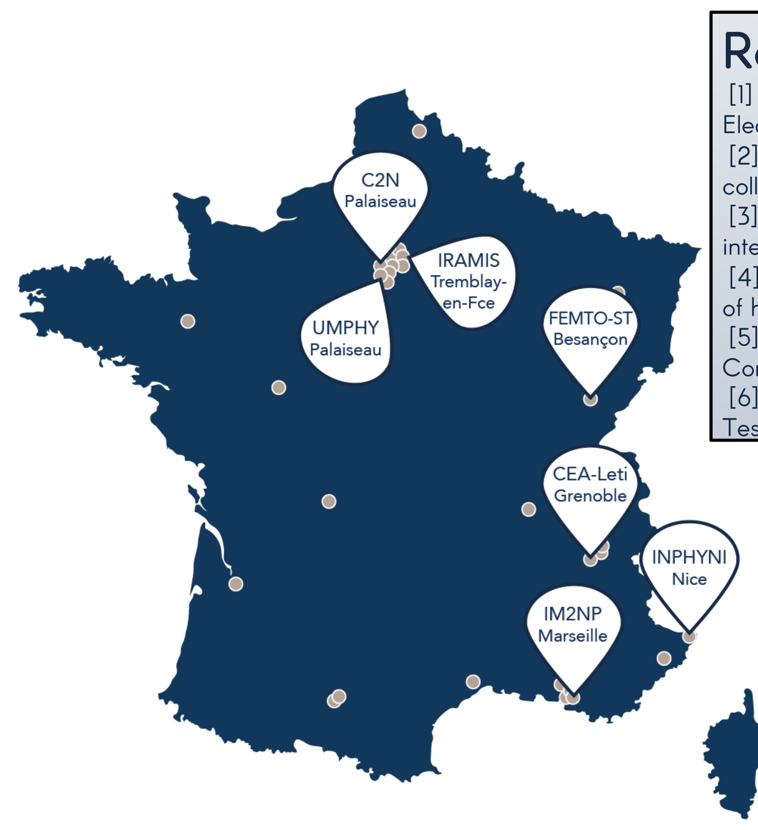
Given that $\boldsymbol{Y}_1$ now becomes the input for the design of layer two, continue this guide iterative approach, the output for the $\boldsymbol{L}$'th layer is,

$$\boldsymbol{Y}_n = \sum_{(i,j)} \boldsymbol{X}_{n-1\updownarrow}^{(ij)} (\boldsymbol{Y}_{n-1} \otimes \boldsymbol{R}_{n-1}) \odot \boldsymbol{E}_{ij} \boldsymbol{X}_{n-1\leftrightarrow}^{(ij)}$$



Future Research Direction

1. Determine how to decompose an arbitrary linear operation into this layered approach.
2. Fabrication and characterization of the 3D Photonic circuits followed by their integration with Opto-Electronic Chips.



References

[1] : Harabi, KE., Hirtzlin, T., Turck, C. et al. A memristor-based Bayesian machine. Nat Electron 6, 52–63 (2023).

[2] : Mauss, Marcel. "Effet physique chez l'individu de l'idée de mort suggérée par la collectivité." Journal de Psychologie Normale et Pathologie 23 (1926): 653-669.

[3] : Moughames, Johnny, et al. "Three-dimensional waveguide interconnects for scalable integration of photonic neural networks." Optica 7.6 (2020): 640-646.

[4] : Adrià Grabulosa. 3D printed photonic circuits towards efficient and scalable integration of hybrid photonic platforms. Optics / Photonic. Université Bourgogne Franche-Comté, 2023.

[5] : Díaz, Josep, Jordi Petit, and Maria Serna. "A survey of graph layout problems." ACM Computing Surveys (CSUR) 34.3 (2002): 313-356

[6] : Ababei, Cristinel, et al. "Placement and routing in 3D integrated circuits." IEEE Design & Test of Computers 22.6 (2005): 520-531.

ANR-22-PEEL-00010