Comparison of an Affordable Open-Source Phase Noise Analyzer with its Commercial Counterpart

Philippe De Visme, Joel Imbaud, Andrew Holme, and Fabrice Sthal

***Abstract*— Phase noise refers to the random fluctuations in the phase of a signal, typically caused by various factors such as electronic components, thermal noise, and environmental conditions. Precise measurement and thorough characterization of phase noise are crucial for evaluating the stability of ultra-low phase noise oscillators. Expensive industrial phase noise analyzers can precisely measure the phase noise of ultra-low phase noise oscillators. However, an affordable open-source phase noise analyzer that can be easily set up is currently lacking. The objectives of this paper are to test an open-source phase noise analyzer, the direct digital phase noise measurement bench developed by A. Holme (called AH analyzer in this paper), and compare it to a commercial phase noise analyzer, the 53100A. Multiple simultaneous phase noise measures and noise floors on both analyzers were made in order to highlight their differences. The open-source analyzer performance turned out to be on par with 53100A's performance, except with the measure of ultra-low phase noise oscillators approaching -132 dBc/Hz at 1 Hz frequencies.**

Index Terms— analog-digital conversion, digital signal processing, field programmable gate arrays board, open source software, oscillator, phase noise, phase noise analyzer, noise floor

I. Introduction

THERE are several methods of measuring phase noise. The simplest and oldest technique is the direct spectrum technique. The signal from the Device Under Test (DUT) is input into a spectrum/signal analyzer tuned to the DUT frequency, directly measuring the Power Spectral Density (PSD) of phase noise in the oscillator [1]. This method has numerous drawbacks, as it cannot distinguish Amplitude Modulation (AM) noise from phase noise and it cannot properly measure close-to-carrier phase noise nor drifting source phase noise. This technique is also limited by the phase noise contribution of the spectrum analyzer being used. The direct spectrum technique is commonly used to estimate the phase noise of low Q resonators.

Usually, precise phase noise measurements are made by analog techniques [2]. In Fig. 1, the basic block diagram of the analog technique with a Phase-Locked Loop (PLL) is displayed. This technique relies on a double-balanced mixer. The mixer, followed by a low-pass filter, functions as a phase detector. Two inputs, one from the DUT and the other from the reference source, are fed into the mixer. The PLL allows the reference source to be at the same carrier frequency of the DUT and in phase quadrature (90° out of phase). For precise phase noise measurements on DUT signals, the phase noise of the reference source must be either negligible or well characterized. This technique offers the highest sensitivity and broad measurement coverage [3], spanning classically a frequency offset range from 0.01 Hz to 100 MHz. Additionally, this approach is unaffected by AM noise and can handle drifting sources. However, drawbacks include the necessity for a clean, electronically tunable reference source for the PLL. Moreover, the mixer, along with the low noise amplifier, must be calibrated at all frequencies of interest. These two drawbacks make the analog techniques difficult to use correctly.

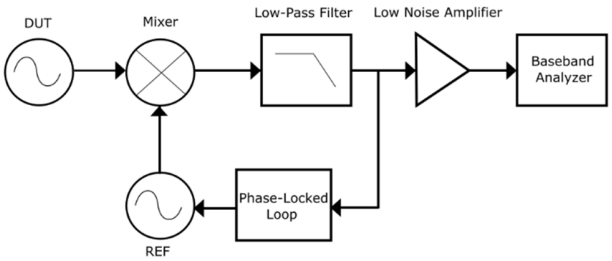

Fig. 1. Analog phase noise measurement technique with PLL.

A recent advancement in phase noise measurement involves a digital technique, as developed in [4]. This method directly samples signals from both DUT and a reference source. The digital phase detection process is carried out through digital signal processing, obviating the requirement for a Phase-Locked Loop (PLL), while digital filters can replace the need for calibration.

Certain commercial phase noise analyzers have adopted this digital technique, with the 53100A from Microchip Technology [5] serving as an example. This analyzer is employed as a reference in this paper. While the 53100A is known as a direct digital phase noise analyzer, its exact architecture remains undisclosed due to it not being an open-source device. The second drawback associated with the 53100A lies in its substantial cost, exceeding $35,000. A. Holme has been working on a low-cost direct digital phase noise analyzer since 2017 (Fig. 2) [6]. This analyzer can be completely rebuilt in-house and costs less than $3,000.

This paper aims to find whether the A. Holme's affordable open-source analyzer (AH analyzer) can have comparable results with an expensive industrial one.

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II. Related Work

There exists several other type of phase analyzers in various applications. Lock-In Amplifier (LIA) is one of them. It allows the extraction of weak signals from noisy backgrounds [7][8]. In this field, Red Pitaya FPGA board can be used to perform the demodulation for low-cost open source LIA [9][10]. Phase noise analyzers are also developed for optical frequency metrology. While the best performances are achieved with FPGA board, the digital signal processing can be done with a more affordable microcontroller unit [11]. Various other phase noise analyzers utilizing the direct digital phase noise measurement method have been developed and investigated. In 2008, a phase noise analyzer utilizing a digital signal processor for the Fast Fourier Transform (FFT) was introduced [12]. However, it exhibited notably high noise floors of -90 dBc/Hz at 1 Hz, emphasizing the necessity for a more efficient digital processing architecture. For instance, FPGA boards could replace the digital signal processing microcontrollers due to their parallel capabilities and higher computational power, which eventually reflects on better numerical resolution and predictability. In 2017, a fully FPGA-based phase noise analyzer [13] was developed using a Xilinx Zynq-ZC706 FPGA board coupled to two pairs of AD9652RF digitizers. This phase noise analyzer succeeded in achieving a noise floor of -127 dBc/Hz at 1 Hz. A. Holme also developed a phase noise analyzer based on an FPGA board. The AH analyzer is capable of measuring sources in the frequency range of [1 MHz, 62.5 MHz]. Later in this paper, we demonstrate that the AH analyzer's noise floor is -130 dBc/Hz at 1 Hz frequency, and it tends to overestimate ultra-low phase noise sources below -132 dBc/Hz. More recently, Yanjun Ma has developed a cost-effective phase noise analyzer named PN2060C [14], utilizing A. Holme's FPGA and C++ source code on dedicated hardware. This system maintains almost the same architecture as the AH analyzer, employing a higher frequency ADC clock of 133 MHz and incorporating a mixer-based down-converter to expand the frequency range to [1 MHz; 200 MHz]. The PN2060C, benefitting from dedicated hardware, is remarkably affordable at only $780. However, it has demonstrated comparable noise floors with the AH analyzer, hovering around -130 dBc/Hz at 1 Hz. Consequently, similar errors to those observed with the AH analyzer should be anticipated when measuring ultra-low phase noise sources.

III. System Architecture

The AH analyzer is composed of a Xilinx SP605 FPGA evaluation kit connected to a Linear Technology DC1525A-A quad ADC evaluation board [15] (Fig. 2). The Xilinx SP605 FPGA evaluation kit has been discontinued but can be replaced by any Xilinx or Altera/Intel FPGA board or even open source FPGA board like the IceStorm project [16] or ULX3S board [17]. The DC1525A-A has been discontinued too but can be replaced by an AD9653-125EBZ.

The AH analyzer uses the digital technique for measuring amplitude and phase noise. In this paper, we will be focused to phase noise. The signals coming from the Device Under Test (DUT) and the reference source are directly converted by ADCs before further processing. The ADCs introduce at least three spurious noises into the measurement: the ADC thermal noise, the ADC quantization noise, and the sampling clock noise. A simple way to reduce the noise caused by the sampling clock is to make a differential measurement noise between the DUT and the reference by subtracting their phases. Then, to cancel the ADC thermal noise and the ADC quantization noise, a cross-spectrum experimental method is used [18] (Fig. 3). It consists of duplicating the measurement using power splitters. The two independent measurements, while containing the same correlated DUT + Reference noise, exhibit different uncorrelated ADC noises. The system will need to have four ADCs and enough correlations to reduce the uncorrelated ADC noises. With these two techniques, the spurious noises coming from the ADCs are successfully reduced.

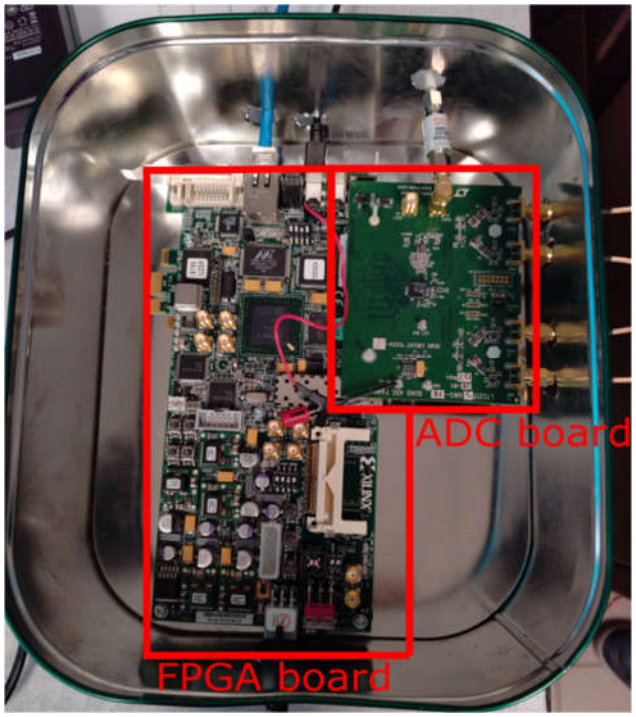

Fig. 2. AH analyzer.

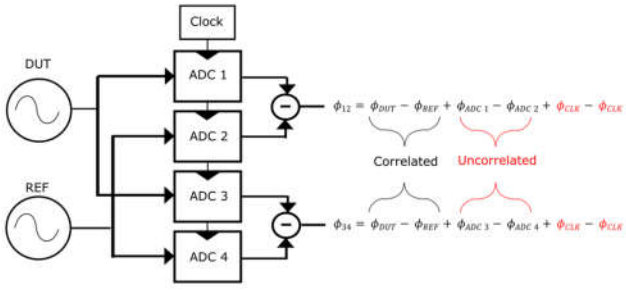

Fig. 3. Cross-spectrum experimental method.

The signals coming from the four ADC channels undergo a series of digital signal processing steps in the FPGA system.

The core of the approach involves a down-converter that follows the sampler. In-phase samples of each input signal are multiplied by the sine and cosine of a synthesized local oscillator and then low-pass filtered. When the local oscillator

frequency is close to the input frequency, the filters' outputs are in-phase (I) and quadrature (Q) base-band samples. The phase difference between the input signal and the synthesized local oscillator is determined using the arctangent function, the Coordinate Rotation Digital Computer (CORDIC) arc-tangent block [19]. This step is crucial to the direct-digital technique. Although the arctangent function is limited to values between -π and +π, phase unwrapping can recover the correct linear function.

The same down-conversion process is applied to the second input channel, and the two results are subtracted to obtain the phase difference between the two sources. If the two input signals have different nominal frequencies, the phase of the second channel must be scaled to match the nominal frequency of the first channel. For instance, when comparing a 10 MHz signal with a 5 MHz signal, the phase difference between the 5 MHz source and the local oscillator must be multiplied by 2 before subtracting it from the phase difference of the 10 MHz signal and its local oscillator. This subtraction process cancels out the phase noise of the instrument's clock oscillator, similar to a dual-mixer phase-difference measurement system. The phase difference is then transformed through FFT into the Single-Sideband PSD, denoted as $\mathscr{L}(f)$, representing half of the power spectral density of phase relative to the carrier, expressed in dBc/Hz. The log/log scale typically spans the frequency range from 0.1 Hz to 100 kHz.

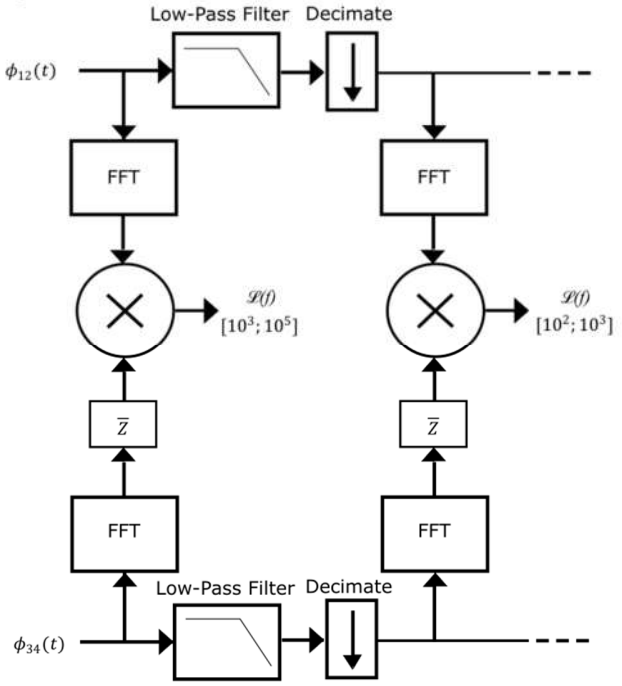

Fig. 4. Architecture of the FPGA signal processing.

To execute these measurements in real-time, the processing stages are divided into a series of identical steps, each decimating by a factor of 10 (Fig. 4). Cross-correlation is introduced in the complex FFT outputs, where bins from one measurement are multiplied by the complex conjugate of corresponding bins from the other. The resulting complex product is averaged over minutes, hours, or days, effectively attenuating uncorrelated noises. Over time, the average real part predominantly contains correlated noise, while the average imaginary part serves as an indicator of the system noise floor.

The signal processing could have been done with a microcontroller instead of the FPGA board. But the FPGA technology is much more suited for this process than the microcontroller. In fact, for this process, averaging can be done in parallels. The FPGA are much more efficient in parallel tasking than a microcontroller [20]. For the microcontroller, the execution speed is limited by the clock speed and the efficiency of the multi-threading or interrupt handling. There is inherent latency in switching between tasks and managing interrupts. Due to their hardware-based parallelism, FPGAs can achieve much lower latency and higher execution speeds. Each logic block can run at the clock speed assigned to it, without the overhead of context switching or interrupt handling. For instance, while one part of the FPGA is handling the acquisition and initial processing of new data, another part can be simultaneously performing averaging on previously acquired data sets.

IV. Experimental Set-up

To compare the two analyzers, a series of $\mathscr{L}(f)$ measures, were made with the experimental setup. These measures were made simultaneously on the AH analyzer and the 53100A (Fig.5), guaranteeing the same measurement conditions. Subsequently, a series of noise floors was conducted on both analyzers to further emphasize the differences between them (Fig 6).

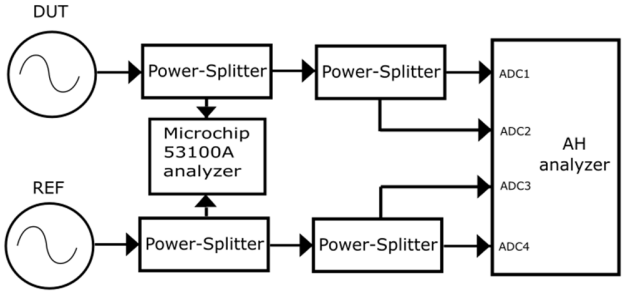

Fig. 5. Simplified schematic of the PSD measure setup.

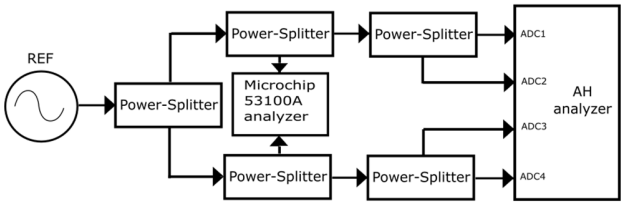

Fig. 6. Schematic of the noise floor measurement setup.

Several sources were used, serving either for DUT or as a reference. All sources must have their frequency within the frequency range of both analyzers. The DC1525A ADC board of the AH analyzer can work up to 125 MHz. Thus, the AH analyzer can measure the phase noise of oscillators up to 125/2 = 62.5 MHz (Shannon). The 53100A can measure oscillators up to 200 MHz. Both the analyzers cannot measure the phase noise of oscillators below 1 MHz. Therefore, the

sources need to have their frequency in the [1 MHz, 62.5 MHz] range. In this paper, measurements were conducted with sources with different levels of phase noise such as two HSO14 Rakon 5 MHz quartz oscillators, two 10 MHz USO Lab-made quartz oscillators, and two synthesizers from Rohde & Schwarz, a SML01 and a SMA100 were used to perform measurements.

Only a 77.76 MHz sampling clock was used to drive the DC1525A ADC board of the AH analyzer. Instrument-generated spurs from ADC quantization appear when the harmonics of the input signal fall close to the harmonics of the sampling clock. A sampling clock of 77.76 MHz has less harmonics close to the harmonics of a 5 MHz input signal than a 125 MHz sampling clock. As a result, the ADCs clock used in the AH analyzer is a Crystek CPRO33-77.760 crystal oscillator.

V. Measurements

Fig. 7 displays the PSD measurement of the SML01 from Rohde & Schwarz, which produces a 5 MHz signal output categorized as a "high-level phase noise" source. Both the 53100A and AH phase noise analyzers measured the SML01 phase noise. The ultra-low phase noise HSO14 Rakon 5 MHz oscillator serves as the reference for both phase noise analyzers. The duration of the measurement is about 18 hours to obtain a good resolution close to the carrier.

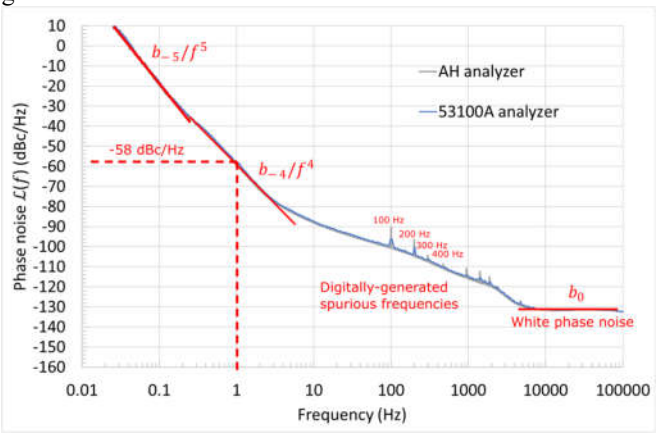

Fig. 7. PSD measures of the SML01 synthesizer from Rohde &Schwarz with both 53100A and AH analyzers with 5 MHz Rakon reference and 1dBm input power.

When assessing "high-level phase noise" oscillators, there are minimal differences observed between the AH analyzer and the 53100A. The two curves show a very close match overall. Although there is a slight variance in the intensity of spurious peaks around 100 Hz. These spurious frequencies appear due to supply voltage which have a frequency of 50 Hz in France. Thus, harmonics (100 Hz, 150 Hz, 200 Hz, …) and sub-harmonics (25 Hz, …) of the main frequency cannot be totally suppressed in noise measurements.

Moving to Fig. 8, which depicts the PSD measurement of a 10 MHz quartz oscillator by both the AH analyzer and the 53100A using an HSO14 Rakon 5 MHz reference source over a 2 hours period, we notice a marginal difference of 2 dBc/Hz along with several spurious peaks around 10 Hz. These spurs were only measured on the AH analyzer during short measures of 2 hours or less. Longer measures allow these peaks to be eliminated by the averages and the correlations. Thus, these spurs do not come from the DUT source or the reference source, or the two analyzers regardless of the duration of the measurement would measure them. This measurement underscores either the disparity in data collection speed between the two analyzers or the capacity of the 53100A analyzer to filter the internally-generated spurs. Fig. 8 shows mainly the consequences of too short measures. Among all the short measures we have made, the 10 MHz oscillator DUT was the one that highlight the biggest difference between the two analyzers.

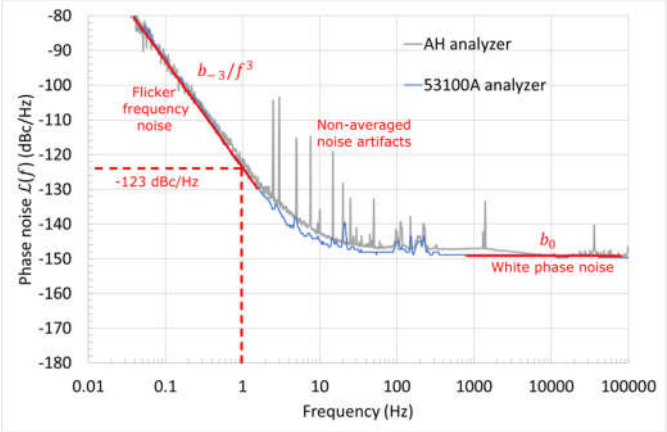

Fig. 8. PSD measures of the 10 MHz oscillator with both 53100A and AH analyzers with a 5 MHz quartz oscillator reference and 1 dBm input power.

Considering these factors, subsequent measurements were conducted for a minimum of 24 hours. with the incorporation of amplifiers to boost the input power to 90% of the maximum capacity.

The following phase noise measurement involves measuring an ultra-low phase noise oscillator. By utilizing two HSO14 Rakon 5 MHz oscillators—one at the DUT input and the other at the reference input of an analyzer—we attribute half of the resulting PSD measurement to each oscillator [21] (i.e. -3 dBc/Hz to obtain the PSD measure of one oscillator). Fig. 9 displays the 24 hours PSD measurement of an HSO14 Rakon 5 MHz oscillator performed by both the AH analyzer and the 53100A, with another HSO14 Rakon 5 MHz oscillator serving as the reference. To enhance the input power, amplifiers AMP77 were introduced, reaching up to 9 dBm (90% of maximal input power of ADC). The 53100A analyzer measures the PSD of the HSO14 Rakon 5 MHz at:

$$\mathscr{L}(1\ Hz) = -128 - 3 = -131\ \text{dBc/Hz}. \quad (1)$$

This result is in proximity to the specifications of the HSO14 (-132 dBc/Hz at 1 Hz [22]). A notable distinction between the two analyzers is that the AH analyzer tends to overestimate the PSD by 5 dBc/Hz in the [0.1 Hz;10 Hz] range.

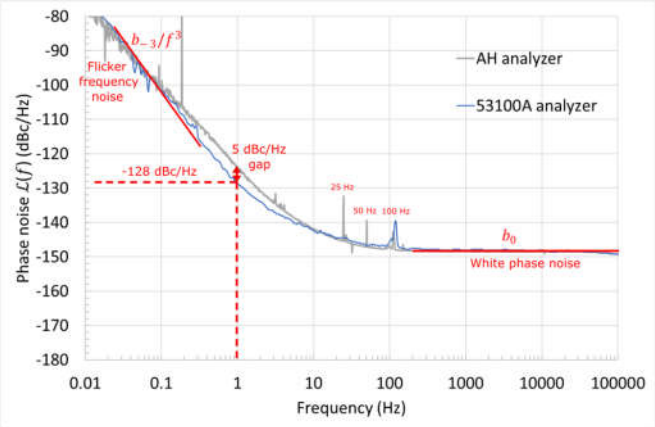

Fig. 9. PSD measures of the 5 MHz Rakon oscillator with both 53100A and AH analyzers with another 5 MHz Rakon reference and 9 dBm input power.

Additional measurements were conducted to understand why the AH analyzer tends to overestimate ultra-low noise sources. Noise floor of both the AH analyzer and the 53100A were done simultaneously. In Fig. 10, an HSO14 Rakon 5 MHz drove the four ADCs inputs of each analyzer for 48 hours. Amplifiers were not used, resulting in a power input of only -2 dBm due to the 7 dBm output of the Rakon 5 MHz minus the about 3×-3 dBm of the power-splitters. The low power input leads to the manifestation of noise artifacts in the PSD observed by both analyzers, with a notable emphasis on the AH analyzer's noise floor.

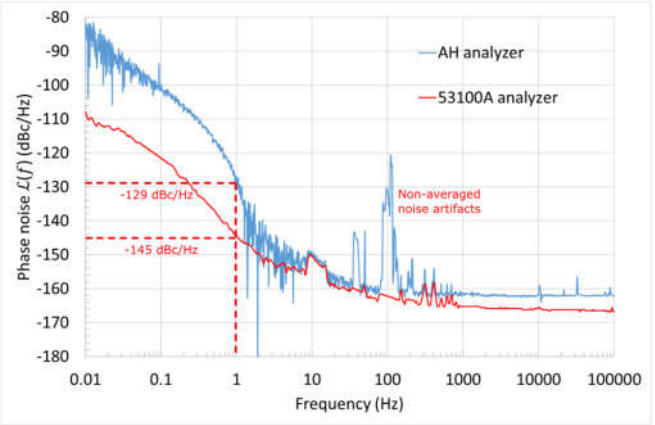

Fig. 10. Noise floor of both 53100A and AH analyzers with a HSO14 Rakon 5 MHz oscillator reference and -2 dBm input power.

To enhance the sharpness of noise floors, one approach is to incorporate amplifiers at the ADC inputs. However, it is crucial to assess whether the phase noise introduced by the amplifiers surpasses the noise floor of the AH analyzer with the HSO14 Rakon 5 MHz as a reference source. In Fig. 11, several noise floor of the AH analyzer with SMA100 synthesizer as reference source are shown.

The SMA100 synthesizer possesses a higher noise floor at low frequencies but demonstrates a lower noise floor at high frequencies [23] compared to the HSO14 Rakon 5 MHz. This feature enables a direct observation of the phase noise level of the amplifiers at high frequencies. Moreover the SMA100 synthesizer have a tunable output power. Therefore, the input power of the amplifiers can be easily changed.

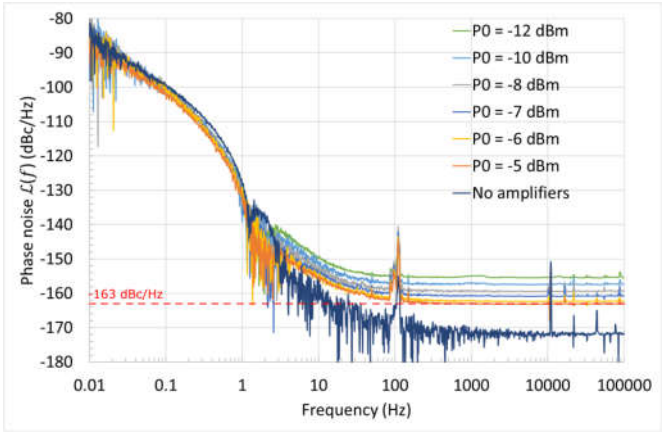

Fig. 11. Noise floor of the AH analyzer with a SMA100 synthesizer reference and AMP77 amplifiers at varying carrier power P_0.

In Fig. 11, the blue curve represents the noise floor of the AH analyzer without the AMP-77 amplifiers with an ADC's input power of 9 dBm obtained with 18 dBm output at the SMA100 analyzer minus the 3×-3 dBm of the power-splitters. Additional curves illustrate the noise floor of the AH analyzer with two AMP77 amplifiers at the ADCs input at varying input power levels. The phase noise originating from white noise in the amplifiers b_0 can be determined using the following formula [24]:

$$b_0 = \frac{F\,k\,T_0}{P_0}. \qquad (2)$$

where F the noise figure of the amplifier (3.3 dB for the AMP77), k the Boltzmann constant, T_0 the temperature (300 K) and P_0 the carrier power (ranging from -13 dBm to -5 dBm). For P_0 = -5 dBm, the noise floor at high frequency is -163 dBc/Hz. This is lower than -162 dBc/Hz, the noise floor of the AH analyzer with an HSO14 Rakon 5 MHz as the reference. Thus, the AMP77 amplifiers can be used with P_0 = -5 dBm to perform the noise floor measurement of the AH analyzer with the HSO14 as the reference without adding noise.

In Fig. 12, a noise floor of the AH analyzer with a HSO14 Rakon 5 MHz oscillator as the reference and two AMP77 amplifiers at the input of the ADCs has been plotted with the 53100A's noise floor of the Fig. 10 and the 53100A PSD measure of the HSO14 of the Fig. 9.

With the inclusion of the two AMP77 amplifiers at the ADC inputs, the noise floor curve of the AH analyzer exhibits a sharper profile. It becomes apparent that the AH analyzer's noise floor is higher than that of the 53100A around the 1 Hz frequency. Moreover, the curve representing the AH analyzer's noise floor is close to the phase noise curve of the HSO14 Rakon 5 MHz oscillator. It causes the overestimation observed in Fig. 9. The AH analyzer due to its high noise floor will overestimate sources approaching -132 dBc/Hz at 1 Hz

frequency.

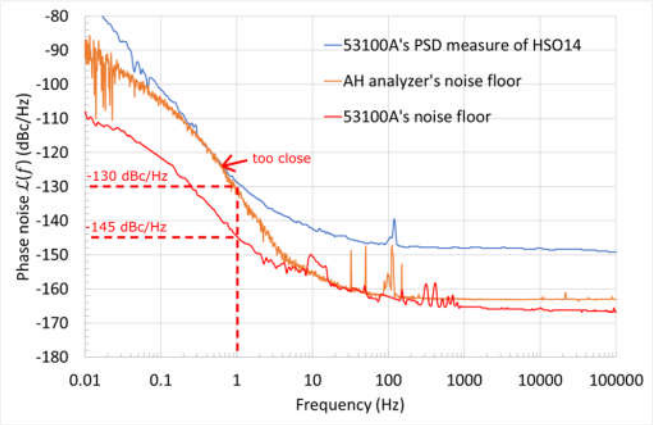

Fig. 12. Noise floor of the AH analyzer with a HSO14 Rakon 5 MHz oscillator reference and a 9 dBm input power ($P_0 = -5\ dBm$) compared with 53100A's noise floor and 53100A PSD measure of the HSO14.

The origins of the phase noise limiting the AH analyzer at low frequencies are not currently known, but some assumptions can be made. Since the FPGA board processes only logic signals, one possibility is that the observed noise floor is due to the ADC board. The characteristic noises of ADCs, such as additive noise, have been well-documented in the literature. Additive noise, which can be represented as an offset in voltage or current, arises from the thermal noise of resistive elements and the shot and avalanche noise of semiconductor junctions. It is considered the primary source of noise in high-resolution, high-frequency ADCs [25]. This additive noise could account for the noises observed at low frequencies. However, the additive noise of one ADC channel should not correlate with that of another ADC channel, and correlations should eliminate this noise.

Another hypothesis is that the noise originates from the power supply of the ADC board. Since the power supply affects the entire ADC board, its noise would not be eliminated by correlations. Currently, the power is provided by the FPGA board. Future work could involve adding white noise to the power supply to observe the sensitivity of the ADC board to power supply noise.

VI. Conclusion

In this paper, we introduced an affordable direct digital phase noise analyzer compare it with the Microchip 53100A phase noise analyzer. Two significant differences were observed. Firstly, the AH analyzer demonstrated a lower data collection speed, requiring prolonged measurement durations and maximum input power to achieve sharp curves. Secondly, the AH analyzer shows a higher noise floor of -130 dBc/Hz around the 1 Hz frequency, resulting in an overestimation of sources approaching -132 dBc/Hz at this frequency. Despite these differences, the AH analyzer yielded comparable results and emerged as an accessible alternative for precise phase noise measurement within the [1 MHz; 62.5 MHz] range.

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