DEVELOPMENT OF LNOI-BASED PHOTONIC DEVICES BY CHEMICAL MECHANICAL POLISHING

Vineck Kumar Posaria*, Danuka Narasinghege Don, Jean-David Fayssaud, Aiman Zinaoui, Miguel Angel Suarez, Samuel Queste, Laurent Robert, Stefania Oliveri, Ludovic Gauthier-Manuel, Mathieu Chauvet, Nadege Courjal

Université Marie et Louis Pasteur, CNRS, institut FEMTO-ST, F-25000 Besançon, France

vineck.posaria@femto-st.fr

ABSTRACT

Photonic Integrated Circuits (PICs) are emerging as a key technology to address the growing demand for high-bandwidth and energy-efficient data processing systems. Among the various photonic platforms, Lithium Niobate on Insulator (LNOI) stands out due to its wide transparency window and strong second-order optical nonlinearity. In this work, we investigate the use of Chemical Mechanical Polishing (CMP) as a fabrication technique for the development of low-loss photonic integrated circuits on the LNOI platform. The design of optical waveguides and Y-junction structures is presented together with the parameterization of the CMP fabrication process. Numerical simulations and design analysis highlight the potential of this approach to reduce fabrication complexity while maintaining low propagation losses. These results demonstrate that CMP represents a promising technology for the development of integrated photonic devices on LNOI.

KEYWORDS : *Lithium Niobate ; Photonic Intergrated Circuits ; Chemical Mechanical Polishing*

1. INTRODUCTION

Lithium niobate is widely used in integrated optics due to its strong second-order nonlinear susceptibility (χ^2) and large electro-optic (Pockels) coefficient, enabling efficient nonlinear frequency conversion and high-speed optical modulation. It also exhibits a broad optical transparency window extending from approximately 400 nm to 5 µm, allowing operation from the visible to the mid-infrared spectral range.

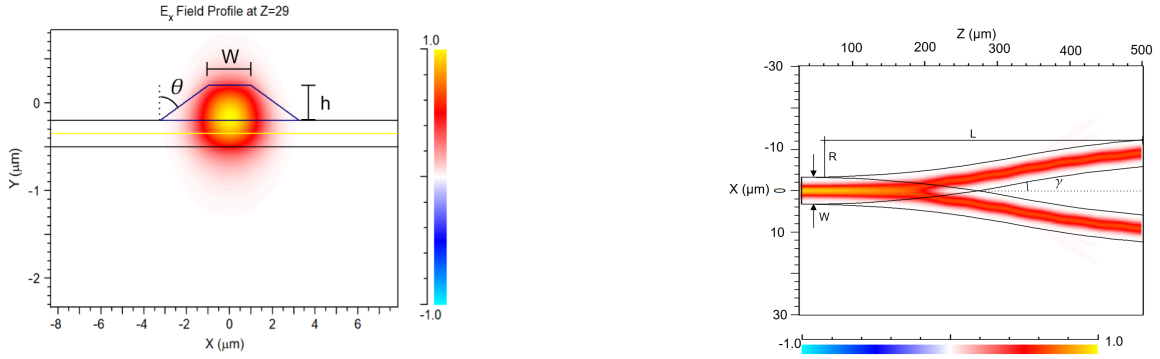
Fabrication of LNOI photonic devices commonly relies on dry-etching techniques such as ICP-RIE or ion beam etching. Although effective, these approaches involve complex processing steps and demanding fabrication conditions.

CMP has recently emerged as a promising alternative fabrication technique[1]. By controlled mechanical polishing, CMP can produce smooth waveguide surfaces while potentially simplifying the fabrication process. In this work, we investigate the feasibility of developing LNOI photonic integrated circuits using CMP, with particular focus on waveguide design and fabrication parameters. Current work explores chromium mask deposition techniques with thicknesses ranging from 200 nm to 600 nm, together with waveguide structures with widths between 1 µm and 10 µm, in order to evaluate the suitability of CMP for low-loss and high-density PIC fabrication.

2. WAVEGUIDE DESIGN AND MASK PARAMETERS

The design of optical waveguides is a critical step in the development of photonic integrated circuits. In this work, the structures under investigation include straight waveguides and Y-junctions, which serve as fundamental building blocks for more complex photonic circuits.

The waveguide geometry is defined by several key parameters. The waveguide width is varied within a range of 1 µm to 10 µm, enabling the investigation of different confinement regimes and



(a) (b)

Figure 1: BeamProp simulations (a) showing mode profile at output of straight waveguide with parameters studied: width, height, sidewall angle) (b) showing propagation in a Y-junction with parameters studied: width, junction radius, junction length, and splitting angle

fabrication tolerances. The waveguide height is targeted between 500 nm and 700 nm, while the sidewall angle is typically designed between 40° and 80°.

For high-density photonic circuits, the spacing between adjacent waveguides is also a critical parameter. BeamProp simulations indicate that the minimum separation required to avoid significant optical crosstalk is approximately 4 μm. Below this distance, modal coupling between neighboring waveguides becomes significant.

The photonic structures are defined using a lithographic mask, where several parameters must be optimized, including mask width and mask thickness. Chromium masks with thicknesses ranging from 200 nm to 600 nm are currently being investigated in order to evaluate their influence on pattern fidelity and durability during the CMP fabrication process.

3. FABRICATION PROCESS USING CHEMICAL MECHANICAL POLISHING

The fabrication process is based on Chemical Mechanical Polishing (CMP), a material removal technique where the wafer is polished on a planarization machine using mechanical abrasion combined with chemical reactions from a colloidal silica slurry [2].

In this approach, a hard mask pattern is first defined on the LNOI wafer. During the polishing process, the mask locally protects the lithium niobate underneath while the exposed regions are progressively removed. As polishing proceeds, the mask pattern is transferred onto the lithium niobate layer, forming the waveguide structures. This technique can produce sub-nanometer surface roughness [3], resulting in very smooth sidewalls and consequently low propagation losses.

An important characteristic of this fabrication method is that the mask thickness directly

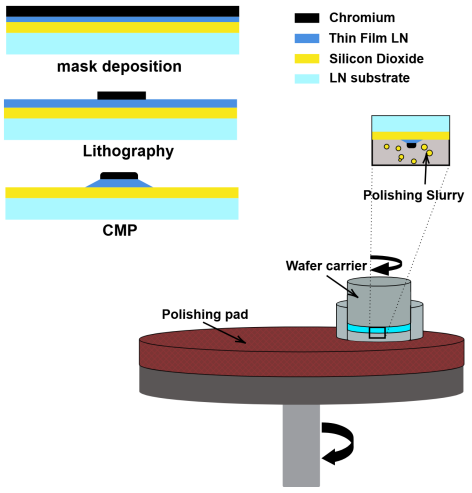


Figure 2: Waveguide fabrication flowchart requires hard mask deposition, lithography and etching of the mask and the CMP step is carried out using a planarization machine that consists of a soft polishing pad and a wafer carrier.

influences the final waveguide geometry. In particular, the mask thickness determines both the waveguide height and the resulting sidewall angle after polishing. For this reason, different chromium mask thicknesses ranging from 200 nm to 600 nm are currently being investigated in order to evaluate their impact on the resulting structures and to optimize the fabrication process.

The CMP process used in this study is defined by several fixed operational parameters:

- Pad rotation speed: 60 rpm
- Carrier rotation speed: 60 rpm
- Applied pressure: 28 kPa
- Slurry type: KOSTROSOL 3550 P

The fabrication process has already been initiated, and current work focuses on optimizing mask deposition and polishing parameters to enable the realization of low-loss waveguides and scalable photonic integrated circuits.

Compared with other LNOI fabrication techniques such as ICP-RIE or ion beam etching, the CMP approach offers the potential for simplified process flows while maintaining state of the art propagation losses.

4. Characterization and simulation results

The fabricated waveguide structures are characterized using an experimental optical setup designed to analyze waveguide propagation and mode profile.

Mode profile simulations performed using BeamProp provide insight into the optical confinement within the designed waveguides. These simulations allow the evaluation of propagation characteristics and support the optimization of geometrical parameters for efficient guiding.
According to reported results in the literature, CMP-fabricated LNOI waveguides can achieve propagation losses as low as 0.28 dB/m [4], demonstrating the potential of this technique for low-loss photonic integrated circuits.

Conclusion

In this work, we investigated the development of photonic integrated circuits on the LNOI platform using Chemical Mechanical Polishing as a fabrication technique. The design of waveguide structures and Y-junctions was presented together with the key parameters involved in mask design and CMP process optimization.

The analysis shows that CMP can significantly reduce fabrication complexity while maintaining low propagation losses, making it an attractive approach for the development of integrated photonic devices. Future work will focus on the fabrication of the designed structures and on the experimental characterization of their optical performance.

References

[1] Richard Wolf, Ingo Breunig, Hans Zappe, Karsten Buse, "Scattering-loss reduction of ridge waveguides by sidewall polishing", *Optics Express*, 2018.

[2] Min Wang, Rongbo Wu, Jintian Lin, et al., "Chemo-mechanical polish lithography: A pathway to low loss large-scale photonic integration on lithium niobate on insulator", *Quantum Engineering*, 2019.

[3] Renhong Gao, Ni Yao, Jianglin Guan, Li Deng, Jintian Lin, Min Wang, Lingling Qiao, Wei Fang, Ya Cheng, "Lithium niobate microring with ultra-high Q factor above 10^8", *Chinese Optics Letters*, 2022.

[4] Rongbo Wu, Min Wang, Jian Xu, Jia Qi, Wei Chu, Zhiwei Fang, Jianhao Zhang, Junxia Zhou, Lingling Qiao, Zhifang Chai, Jintian Lin, Ya Cheng, "Long low-loss lithium niobate on insulator waveguides with sub-nanometer surface roughness", *Nanomaterials*, 2018.